

$$Z = \overline{W} + \overline{X}$$

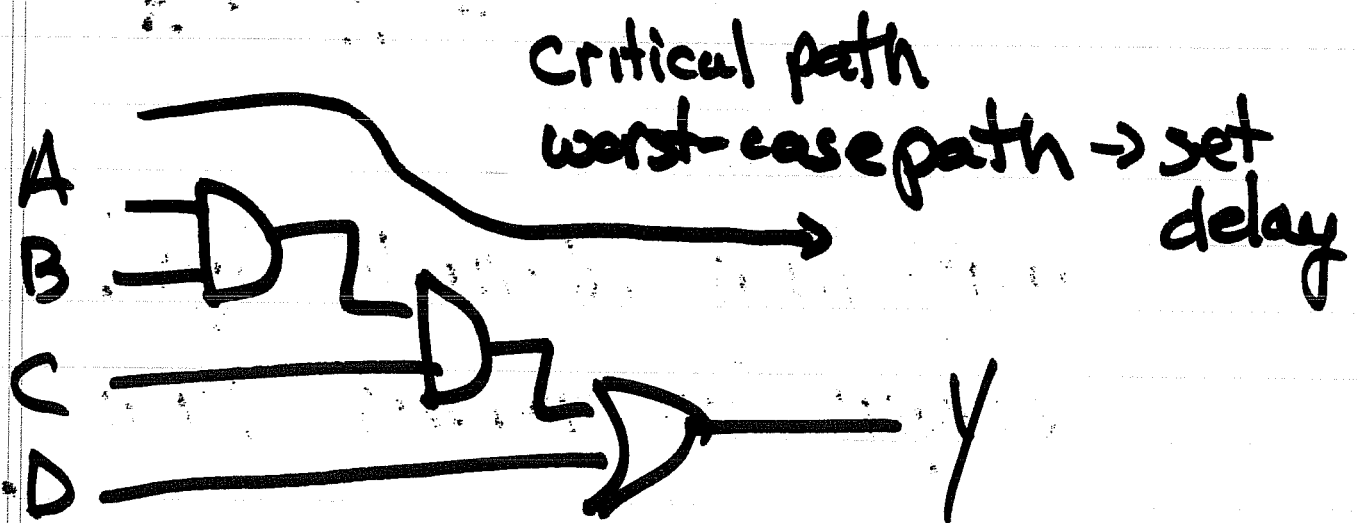
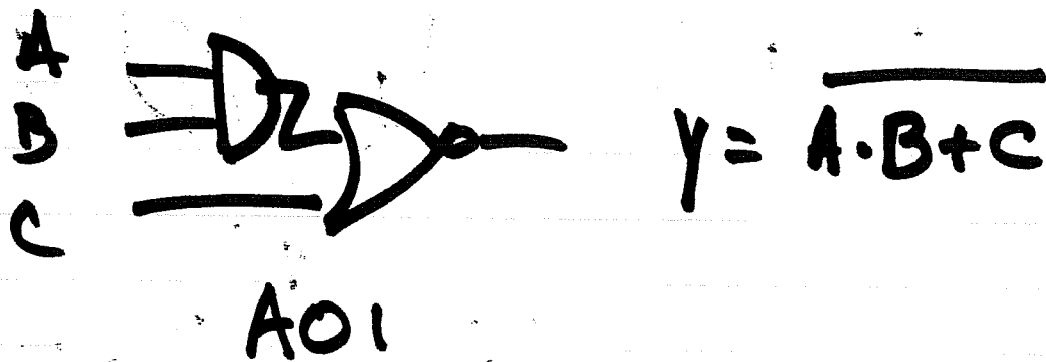
Logic Fan-In will grow
with number of inputs

2-level
K-map

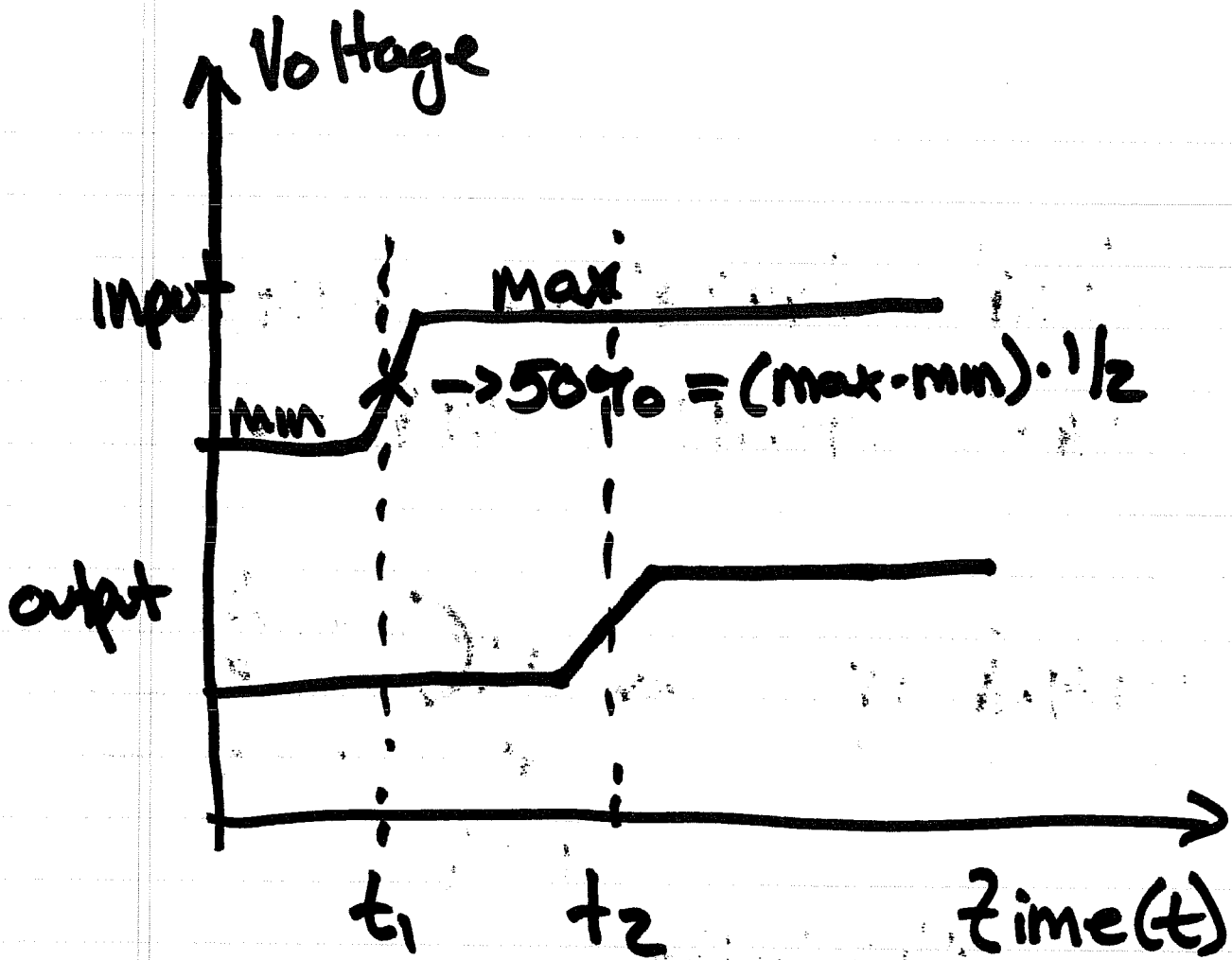
Digital
System
Design

AND-OR-INVERT (AOI)

OR-AND-INVERT (OAI)



Propagation Delay = measure
from input to output at 50%
level

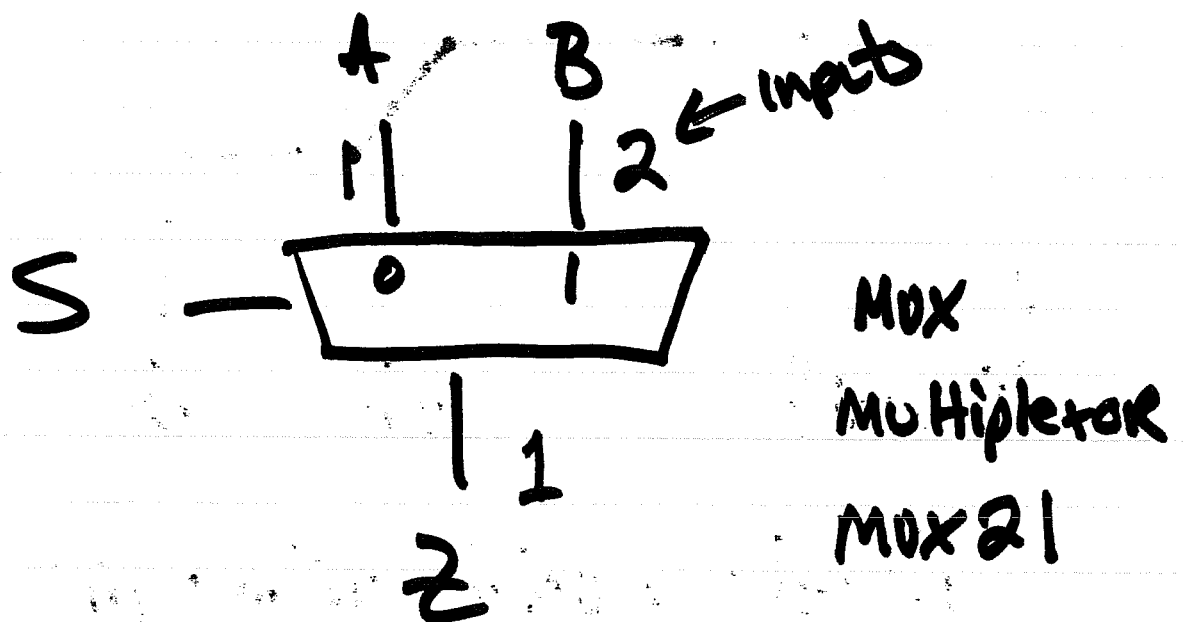


$$\text{Propagation delay} = t_2 - t_1$$

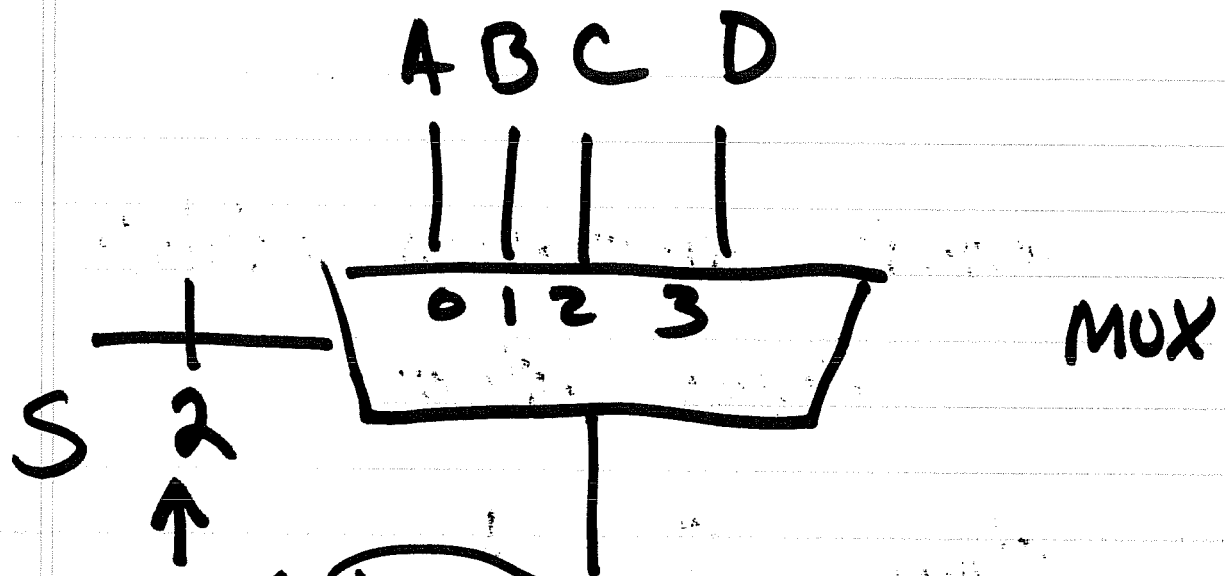
Critical path - worst case prop delay
 from input to output

Contamination delay = minimum
 propagation delay from input to output

glitch = momentary change
in the output



$$Z = A \cdot \bar{S} + B \cdot S$$



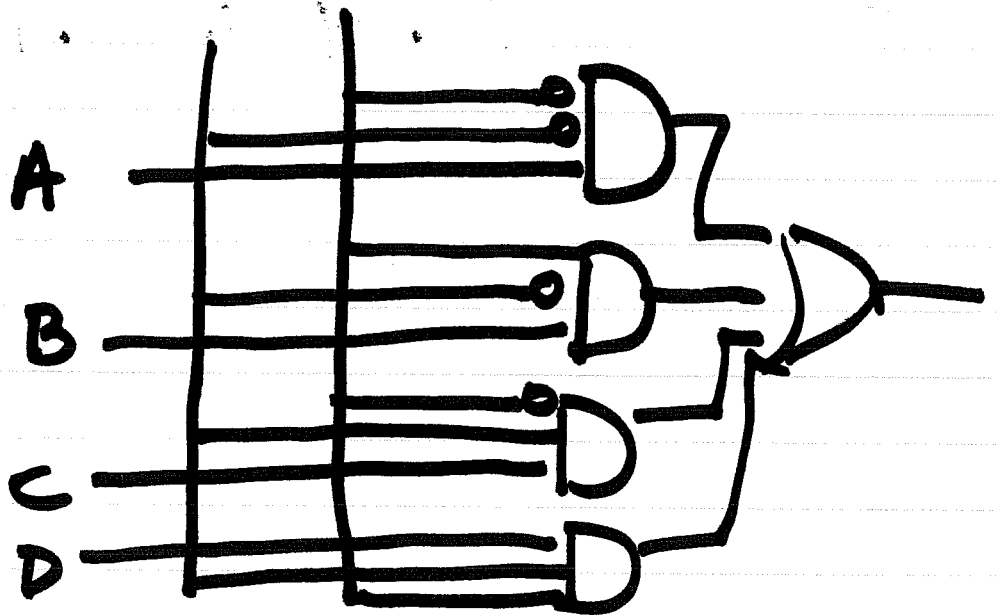
$\log_2(4)$

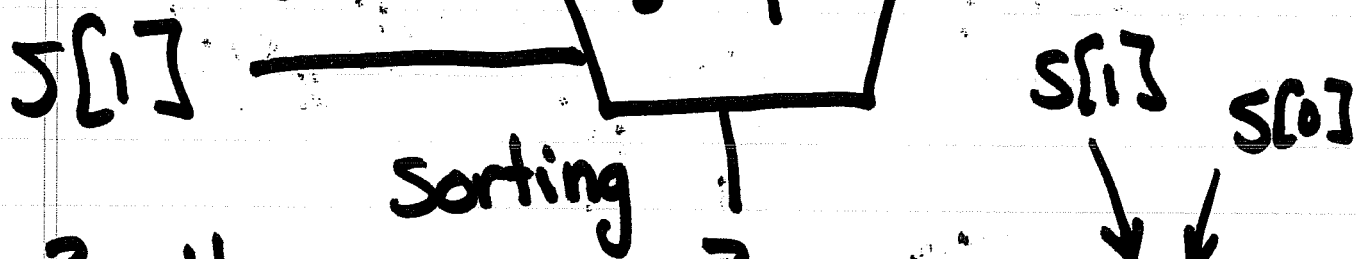
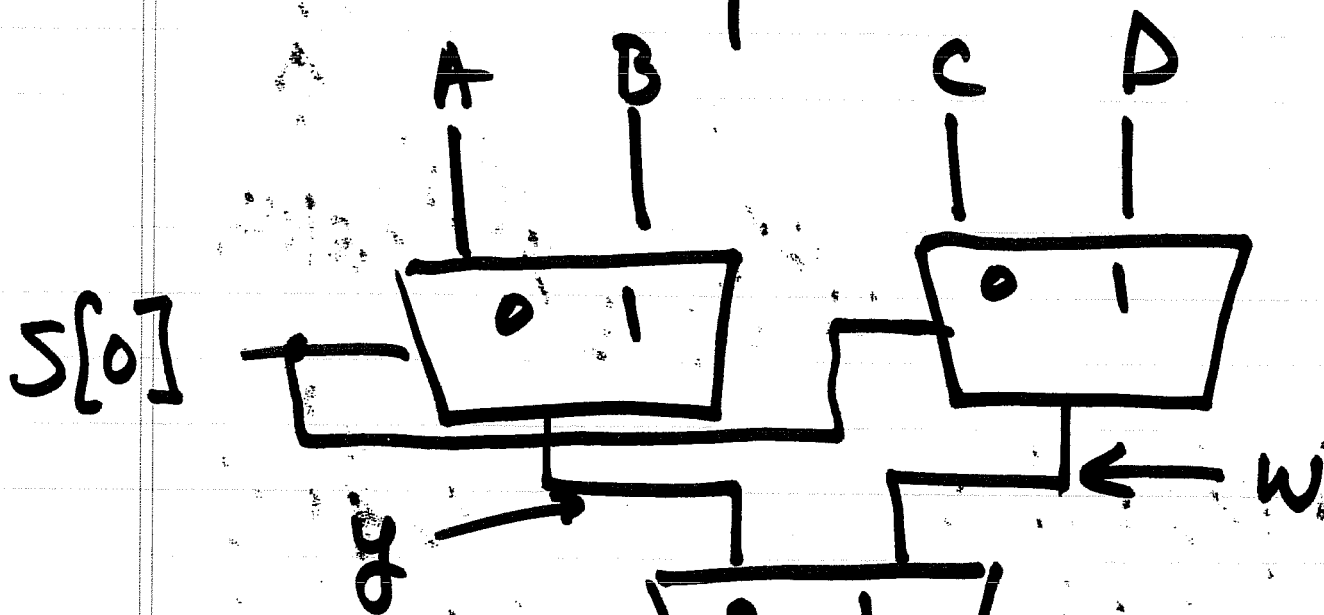
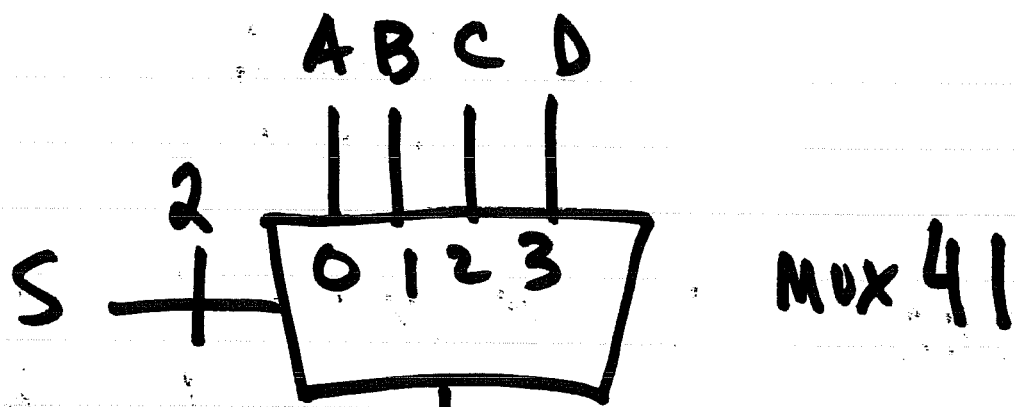
$2^2 = 4$

$\frac{\log_{10}(x)}{\log_{10}(b)} = \log(x, b)$

Excel

S, S₀





$$S = 3 = 11_2$$

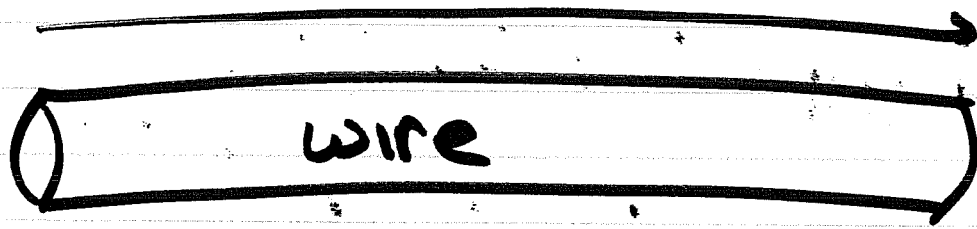
$$Y = B \quad W = D$$

$$z = D \quad \text{☺}$$

$$S = 2 = 10_2$$

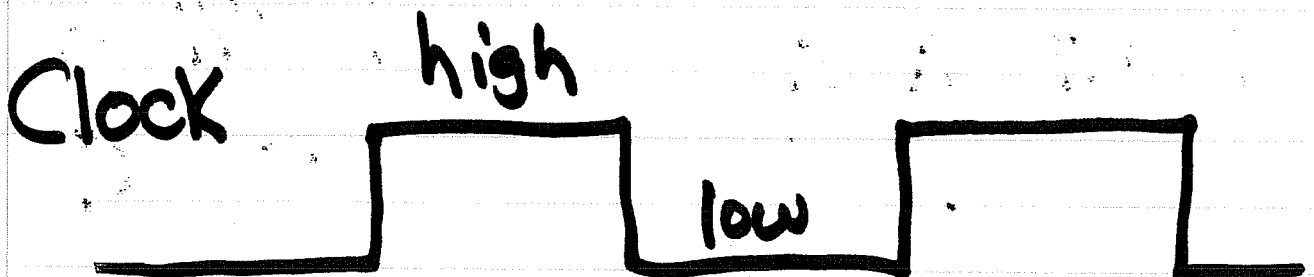
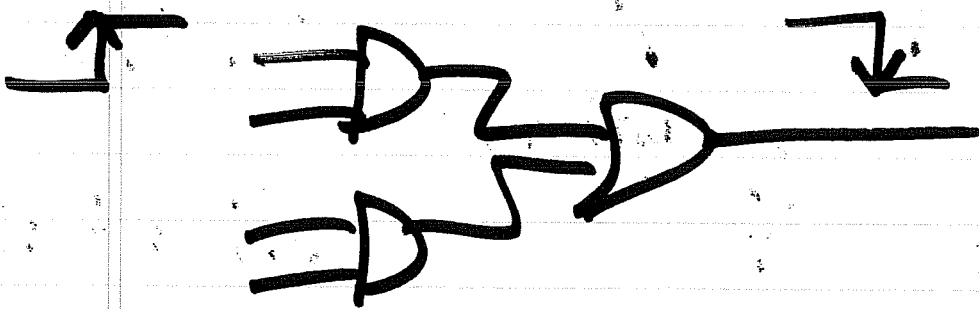
$$Y = A \quad W = C$$

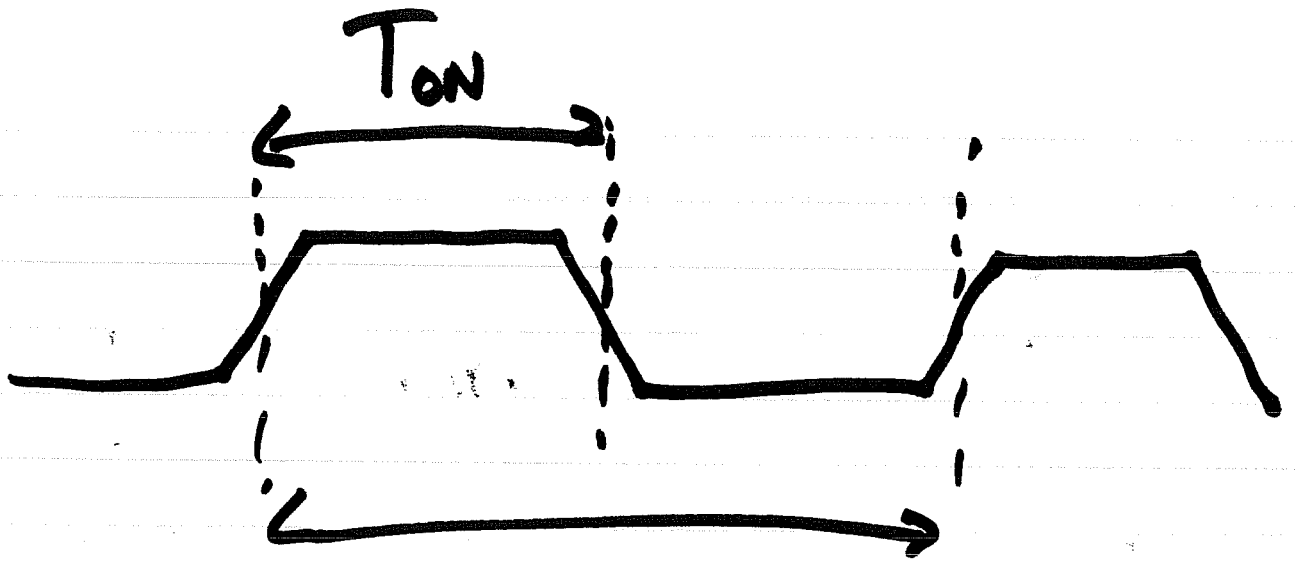
$$z = C$$



Electromagnetic wave travels
at the speed of light

$$2.998 \times 10^8 \text{ m/s}$$





$T_c = \text{cycle time } \& \text{ (period)}$

$$\text{frequency} = \frac{1}{T_c}$$

Pentium IV \cdot 1 GHz \downarrow frequency $T_c = 1 \text{ ns}$
 $1 \times 10^{-9} \text{ sec}$

$$\text{Duty Cycle} = \frac{T_{ON}}{T_c}$$

50% = D.C.

$$v = \frac{1}{\sqrt{\mu\epsilon}}$$

$\mu = \text{permeability}$
 $\epsilon = \text{permittivity}$

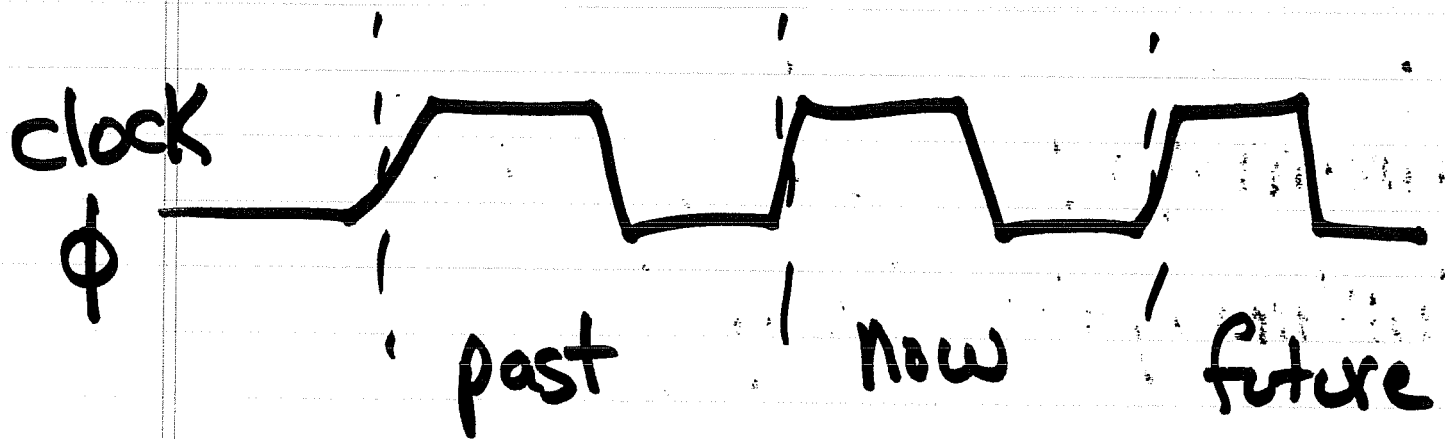
$$t_d = l/v$$

time of travel
through a wire

~~length~~ length (l) will
affect delay

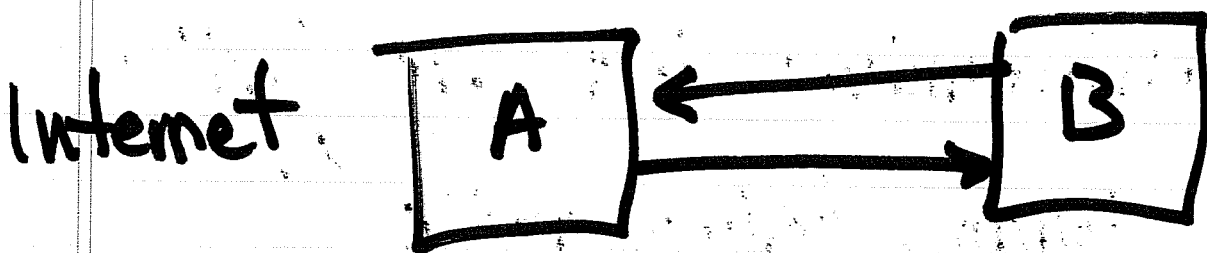
Sequential circuits = all circuits
that are not combinational

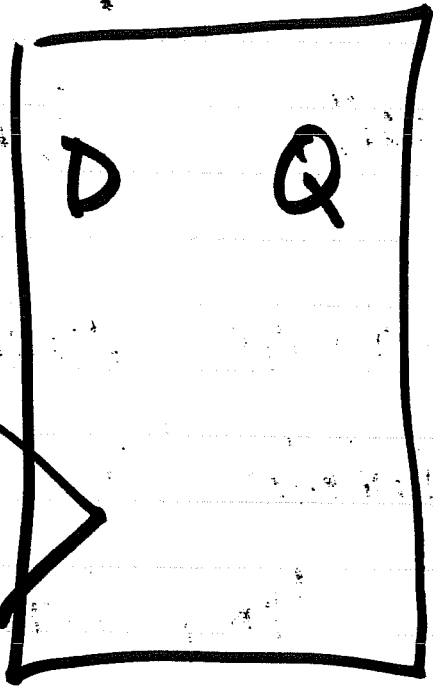
↑ When output cannot be
determined by looking at
current inputs



Synchronous circuits - depend on clock to stabilize now, future, and past

asynchronous circuit - Star Wars technology

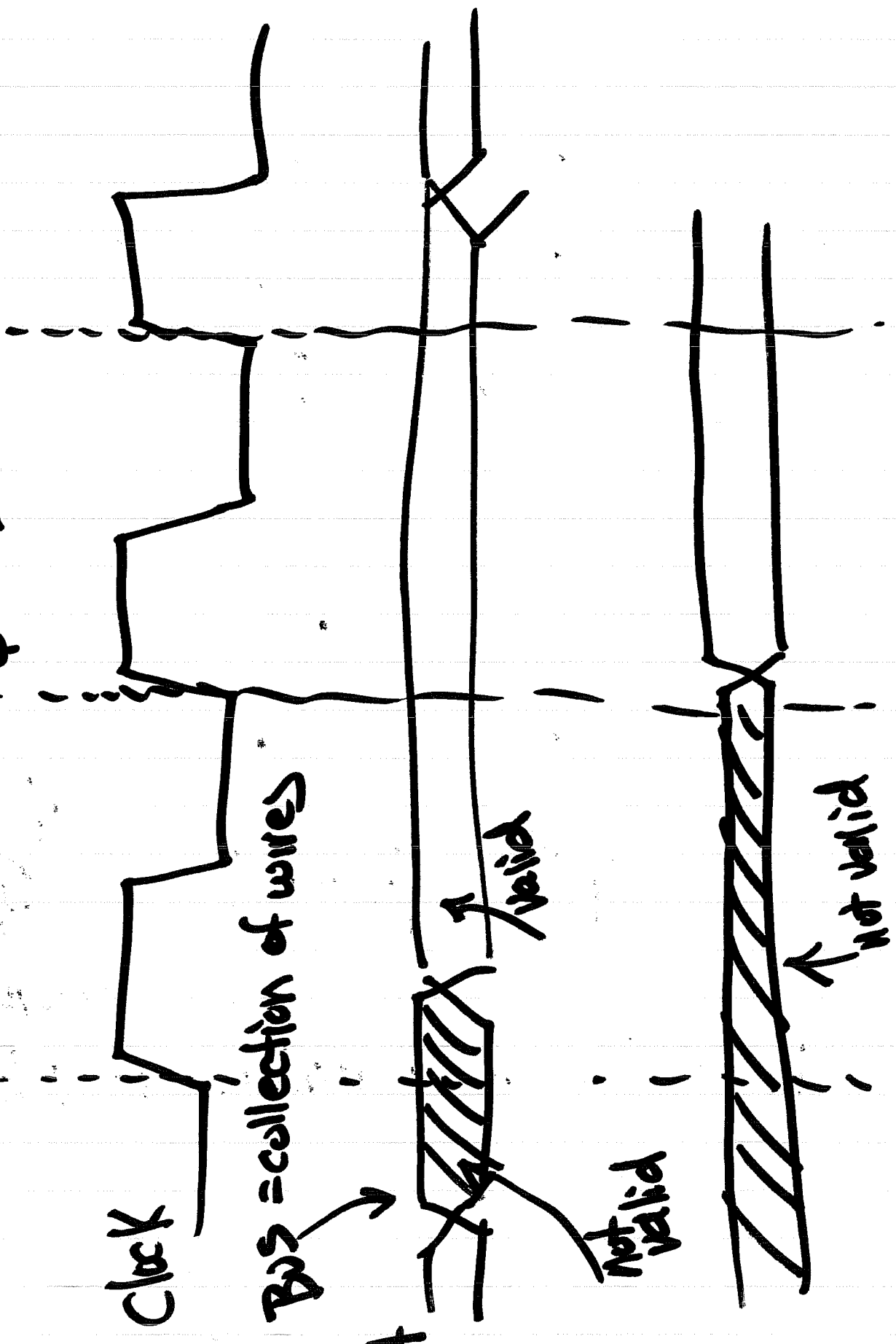
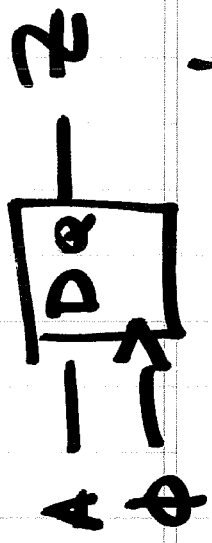




output
will
change

D-flip flop

only on rising edge of clock



Clock

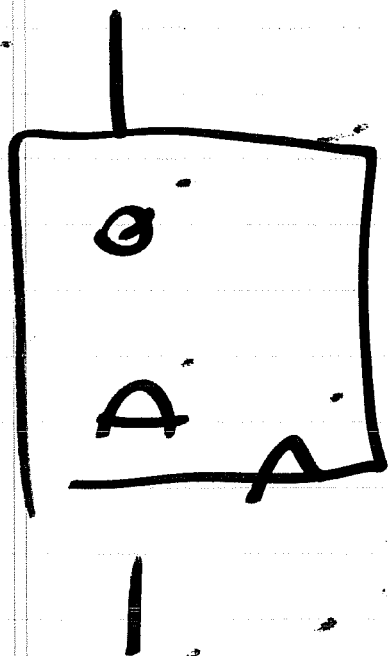
Bus = collection of wires

A

not valid

valid

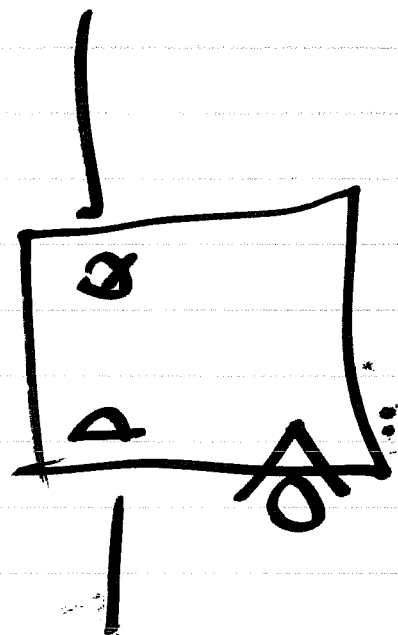
not valid



positive edge

DFF

7474



negative edge

DFF