

# Real World Issues

## De Morgan's Theorem

$$y = \overline{A + B}$$

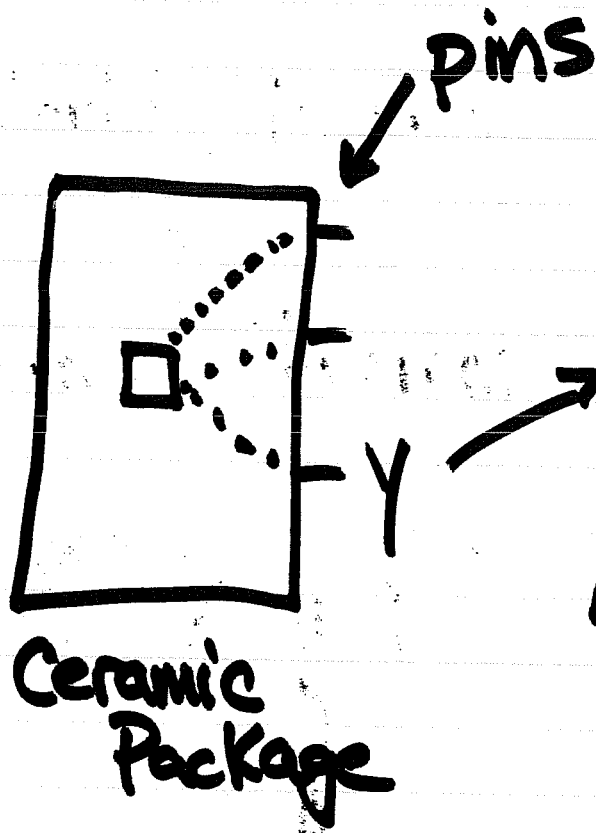
$$y = \bar{A} \cdot \bar{B}$$



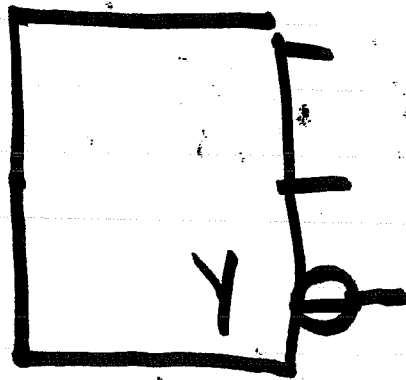
add/  
remove  
bubbles

change type of  
gate

(Materials)  
Ceramic  
Engineering

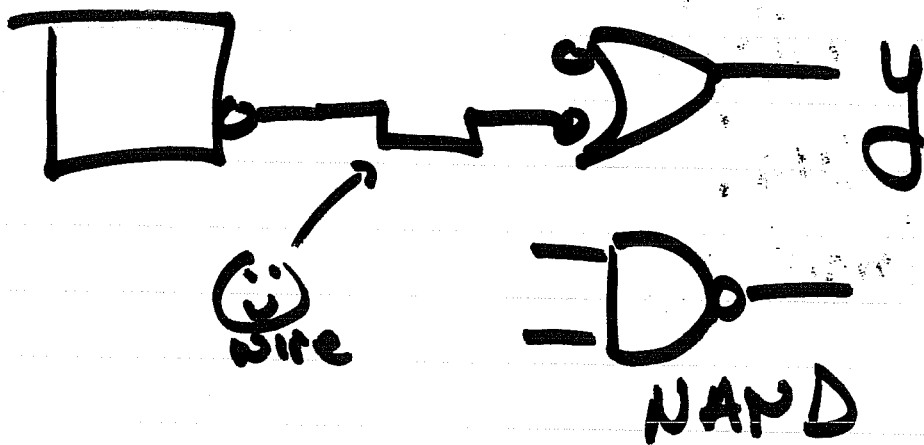
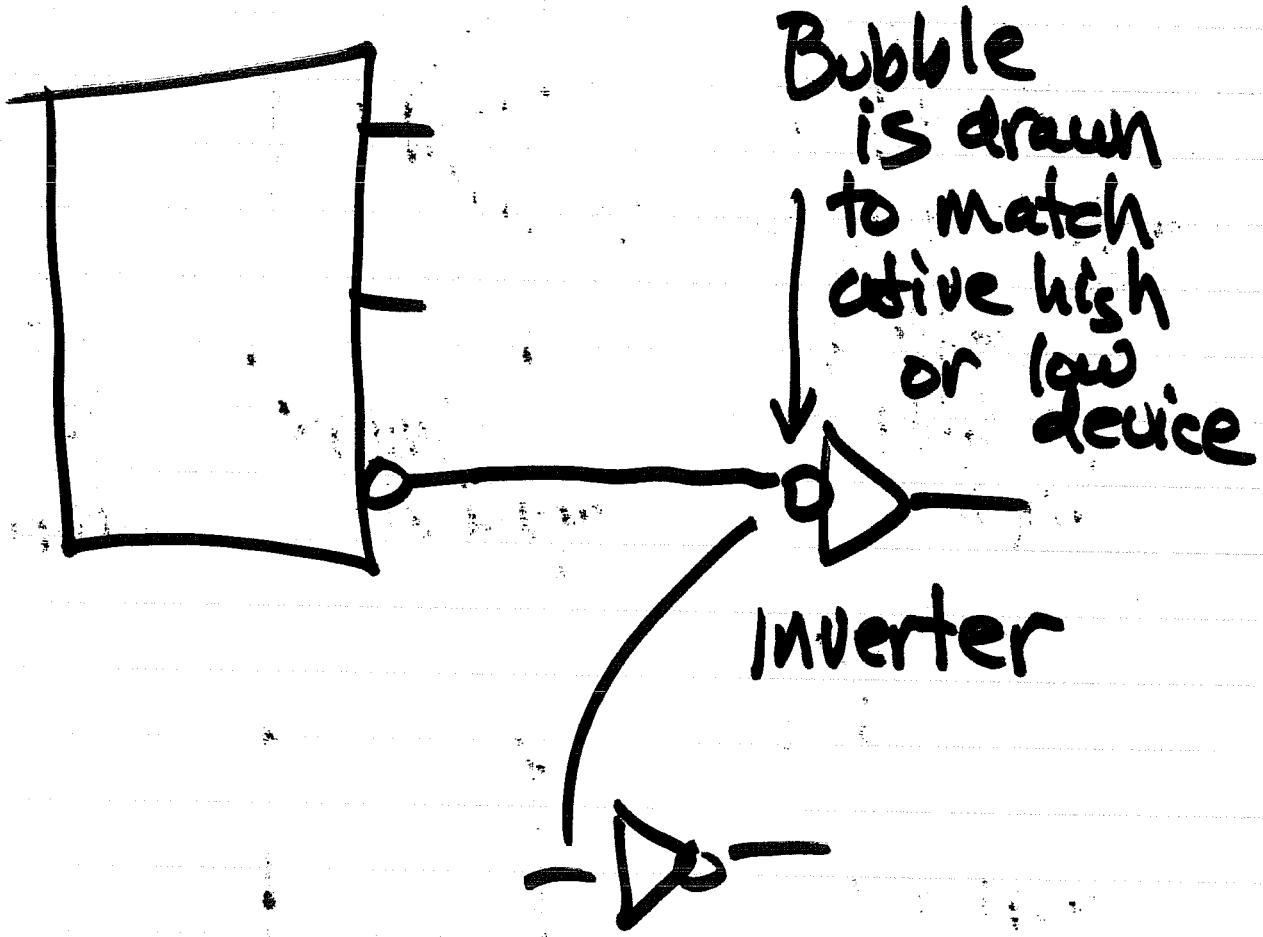


1 = True  
0 = False  
Active  
High  
signal

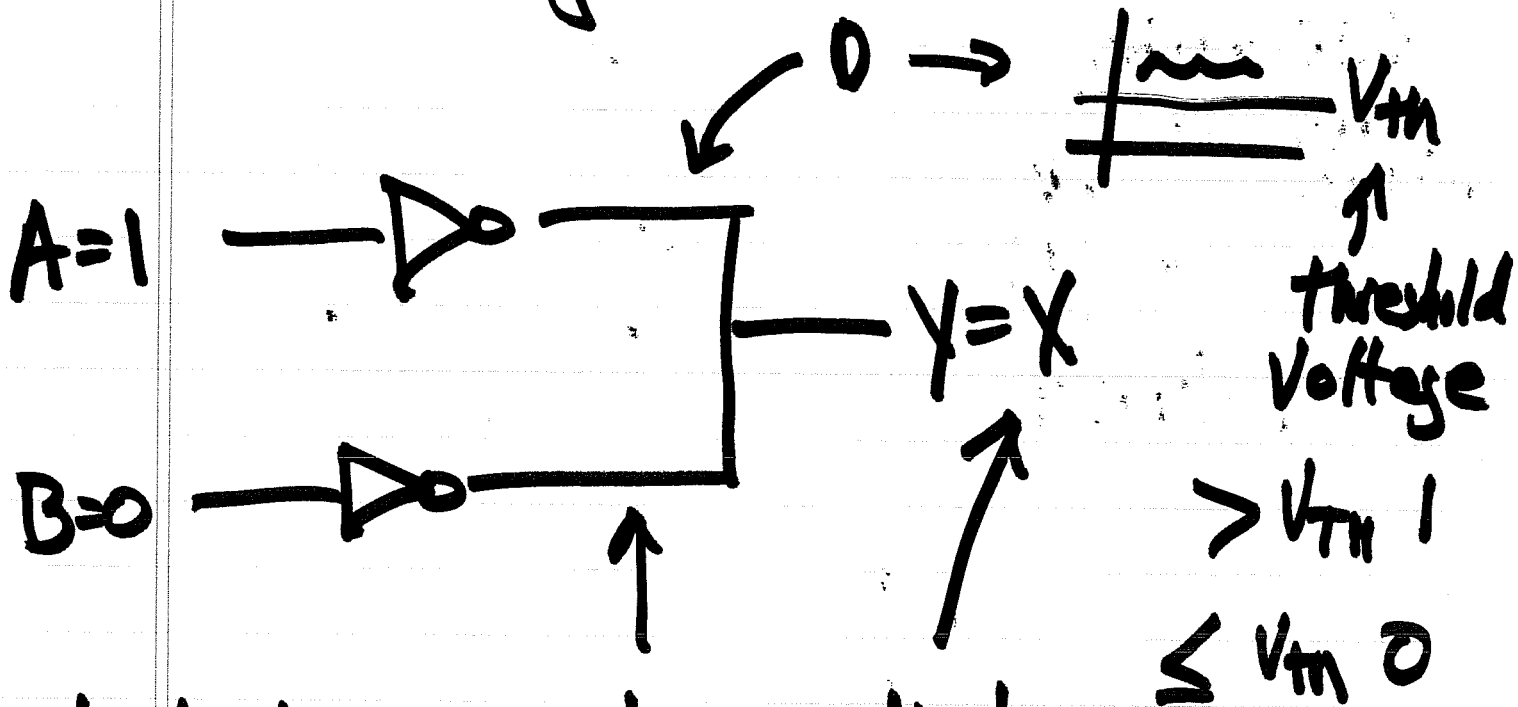


$\overline{Y}$   
0 = true  
1 = false

Active  
Low  
signal

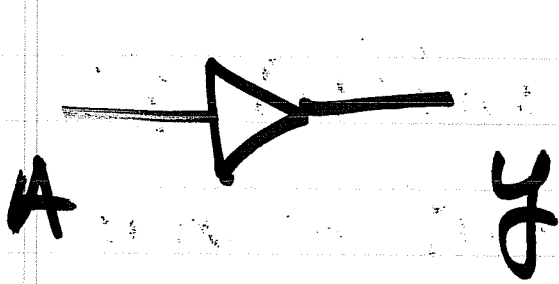


Mr. Ambiguous  $\rightarrow$  In other words, Boolean logic is not always as it seems



Must be avoided!

indicates that the ckt has an unknown or illegal value



Buffer

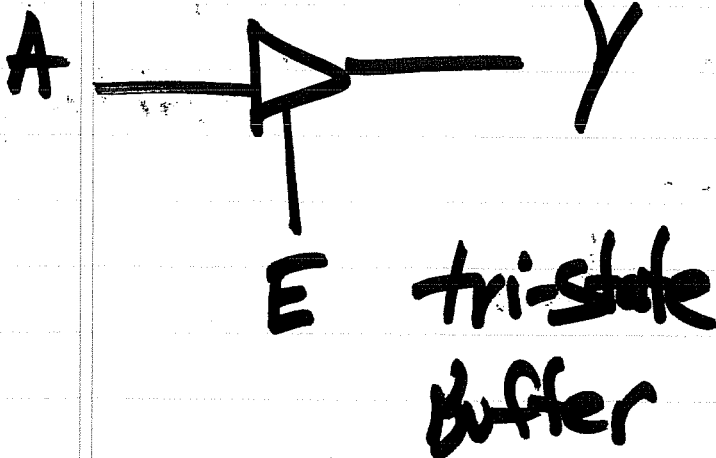
A	Y
0	0
1	1

buffer voltage protection

guarantee an output

74LS04

↳ family

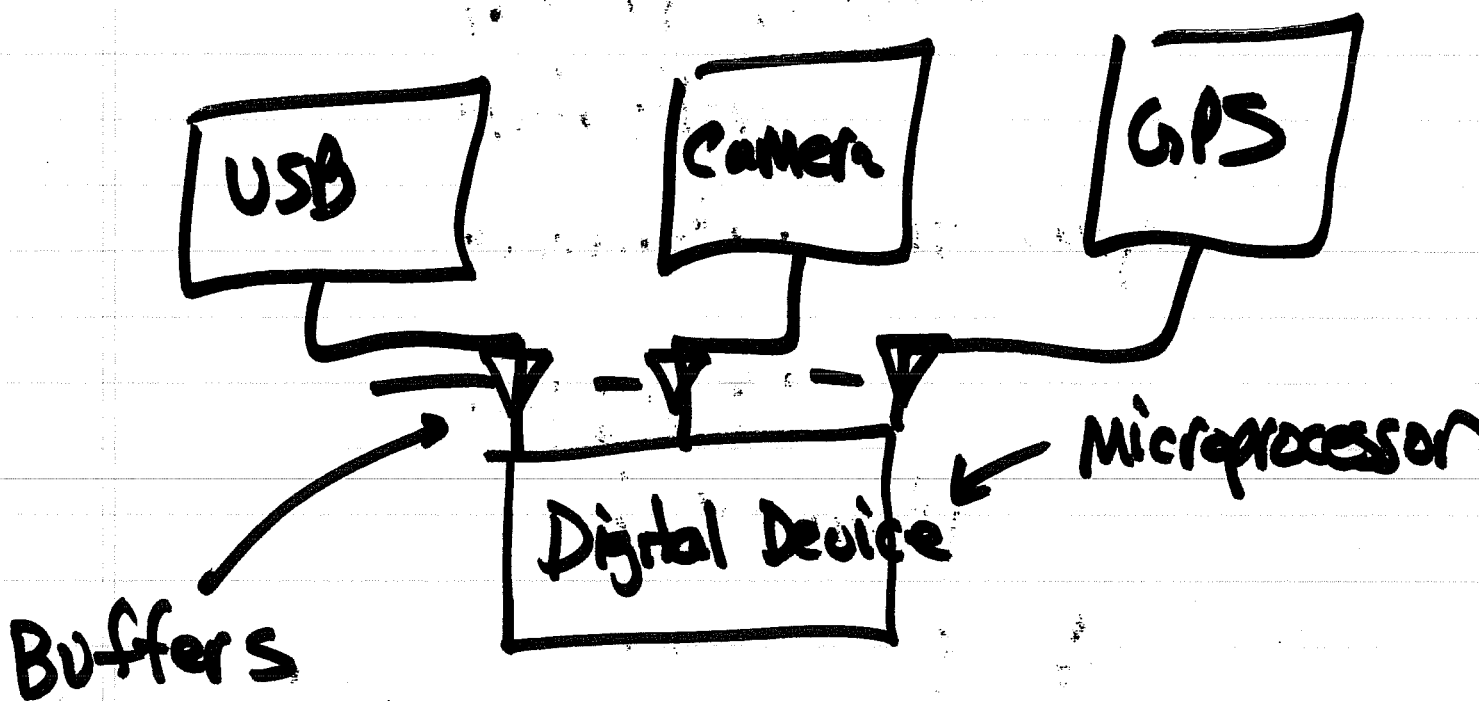


tri-state  
buffer

E	A	Y
0	0	ZZ
0	1	ZZ
1	0	0
1	1	1

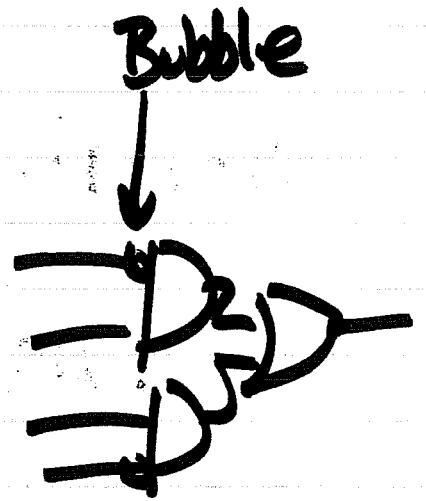
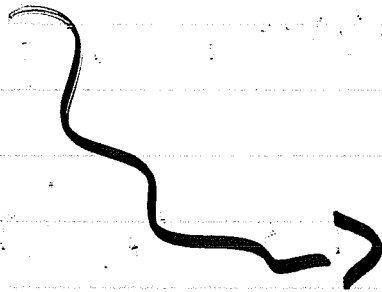
Z-floating value (high impedance value)

Symbol  $\Sigma$  indicates  
a node is being driven  
neither high or low.



or  
tristate buffers can help with  
shared devices

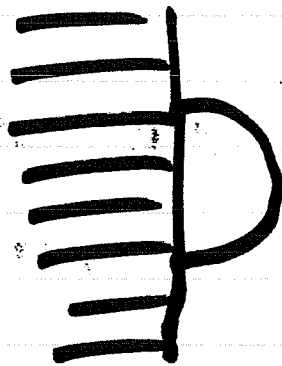
K-map  
TT



2-level  
optimization

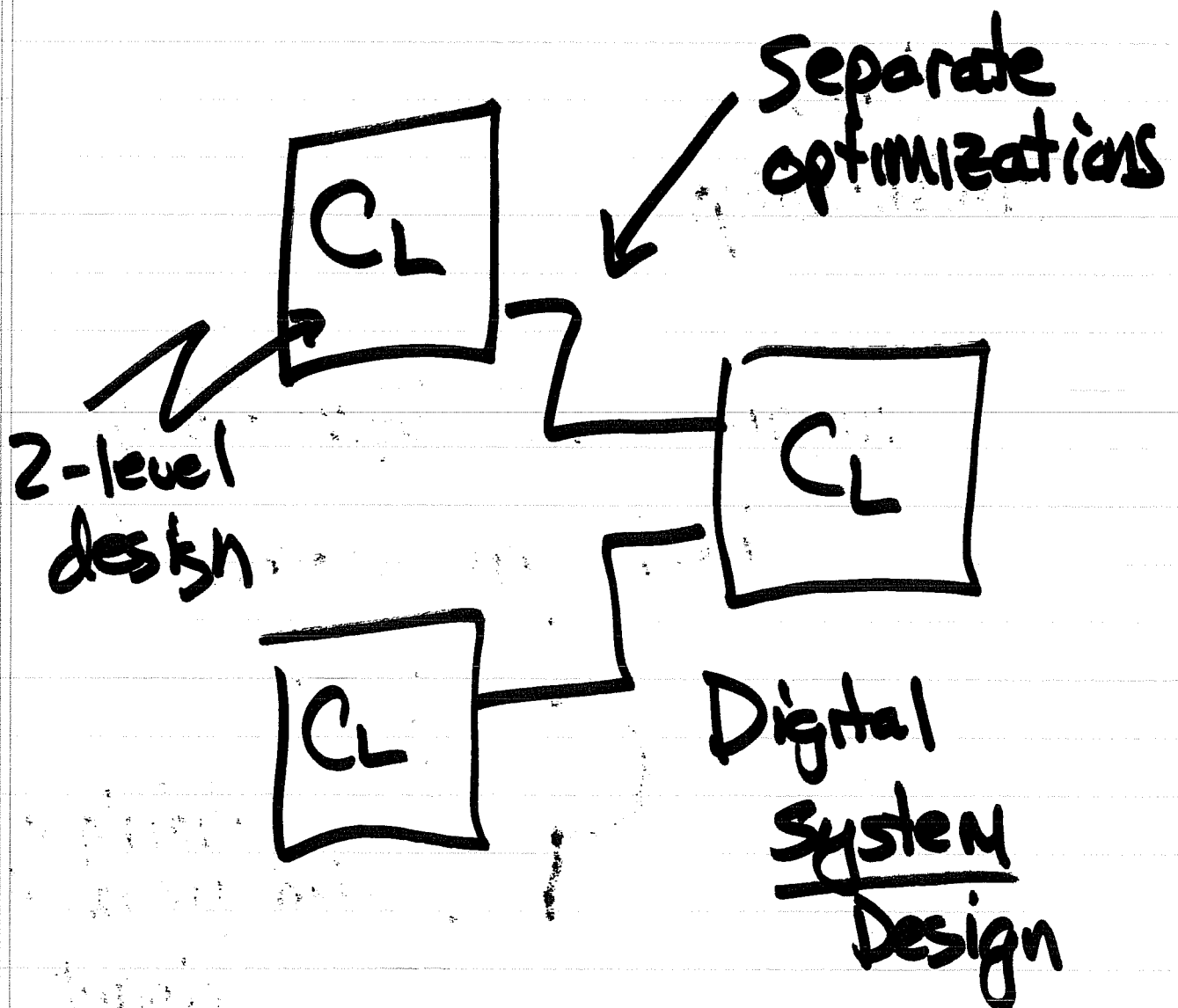
high-input or fan-in  
of gates are bad

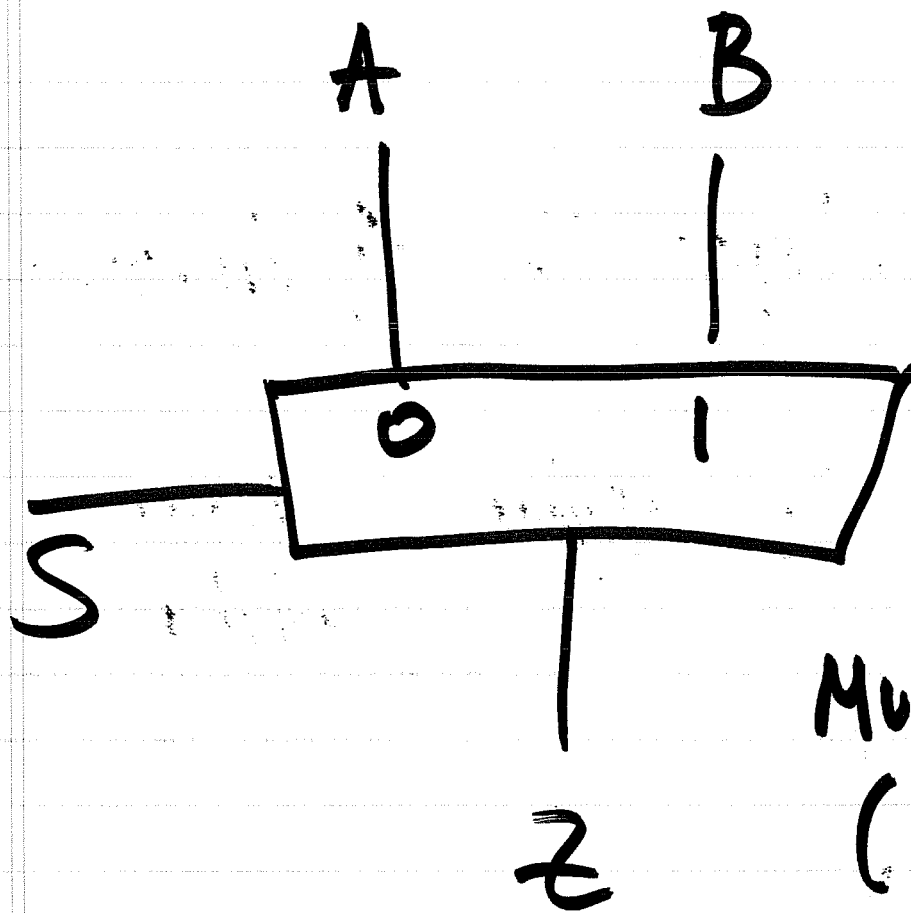
contribute  
to busy (bad)  
signals



fan-in  $\triangleq$  # inputs to a ckt

good advice fan-in  $\leq 4$



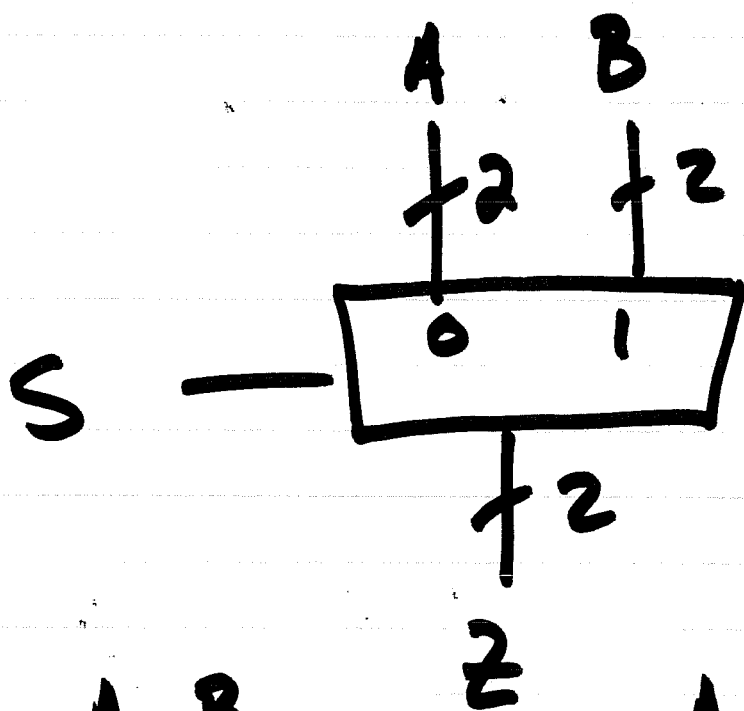


if  $S = 1$   
 $Z = B$

else  
 $Z = A$

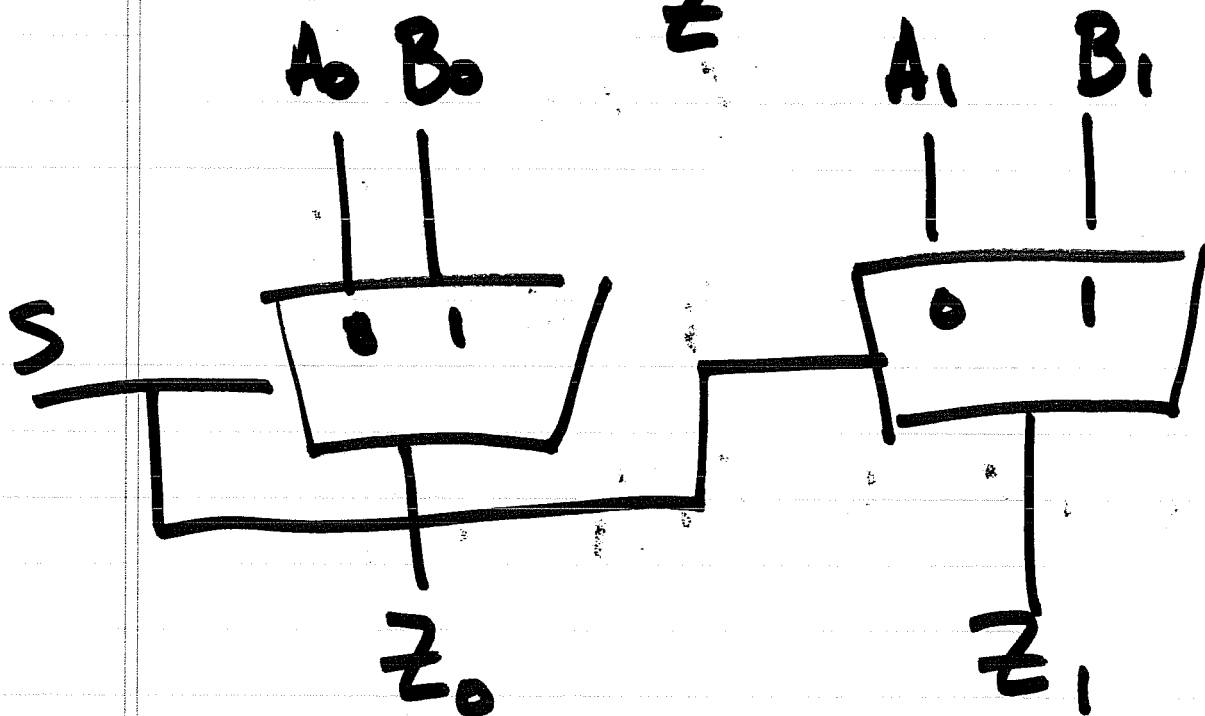
$$Z = A \cdot \bar{S} + B \cdot S$$

What if I needed 2-bits  
for A and B



$$2+2+1$$

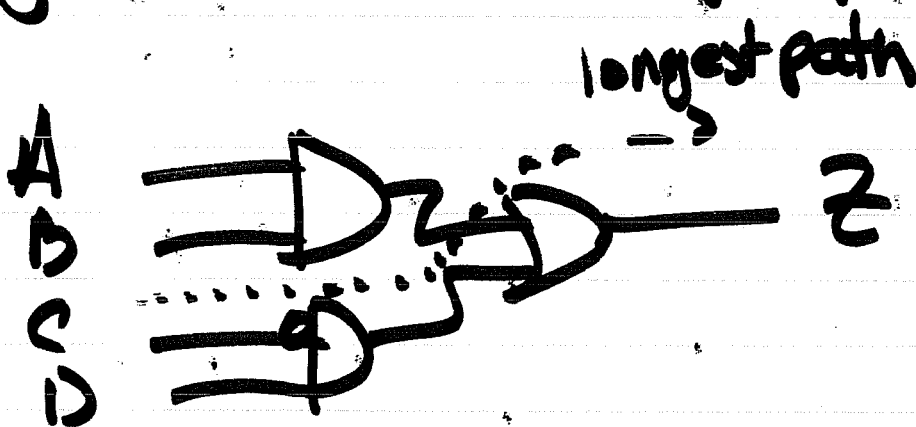
$$\downarrow$$
$$2^5 = 32$$



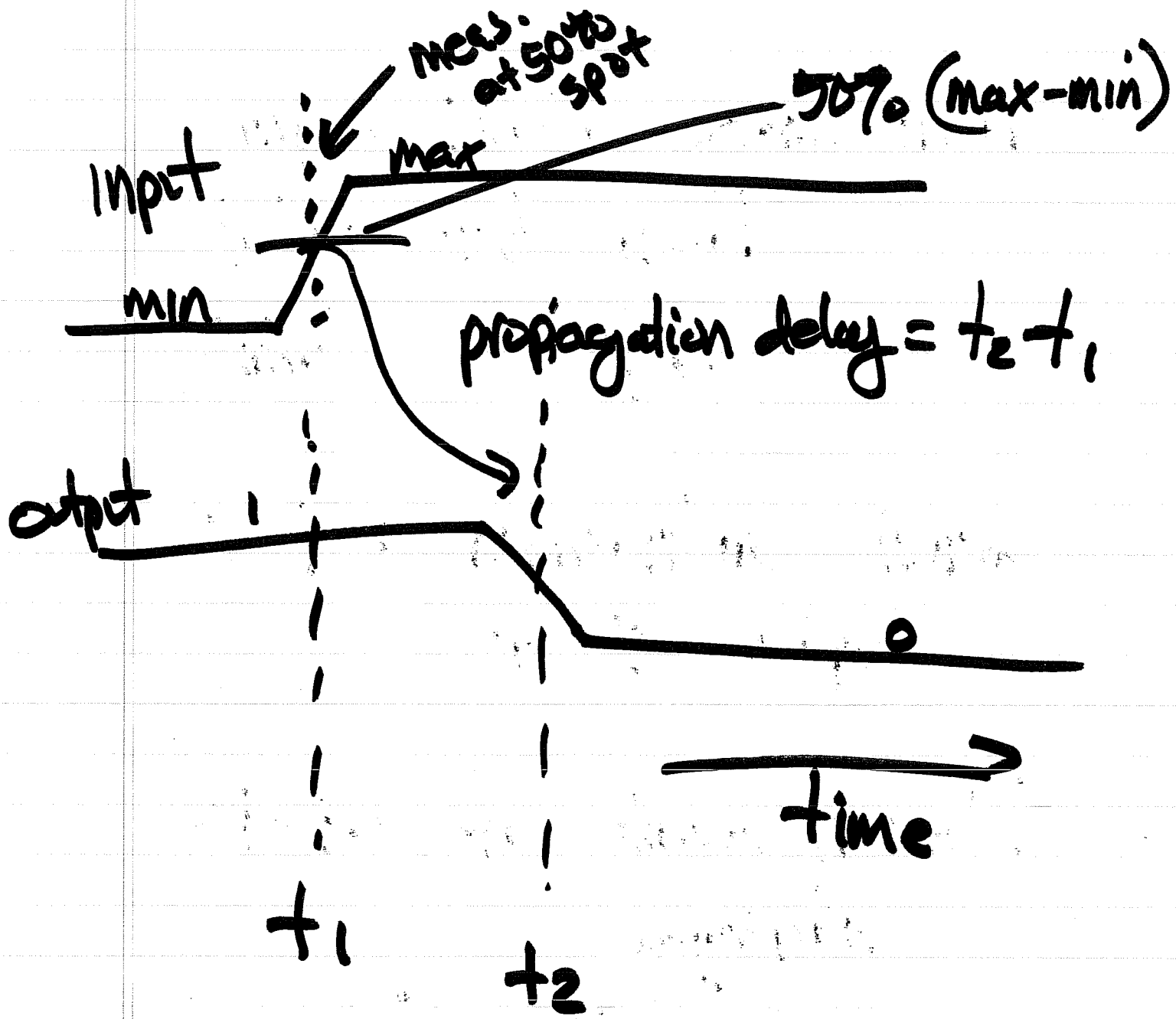
Complex Digital Systems incur  
delay and area!  
(time) (space)

glitch = momentary change  
in the output

glitches are always present!



Critical path = longest propagation  
time or delay from input to output



propagation delay = measured time  
 from input to output at 50%  
 level