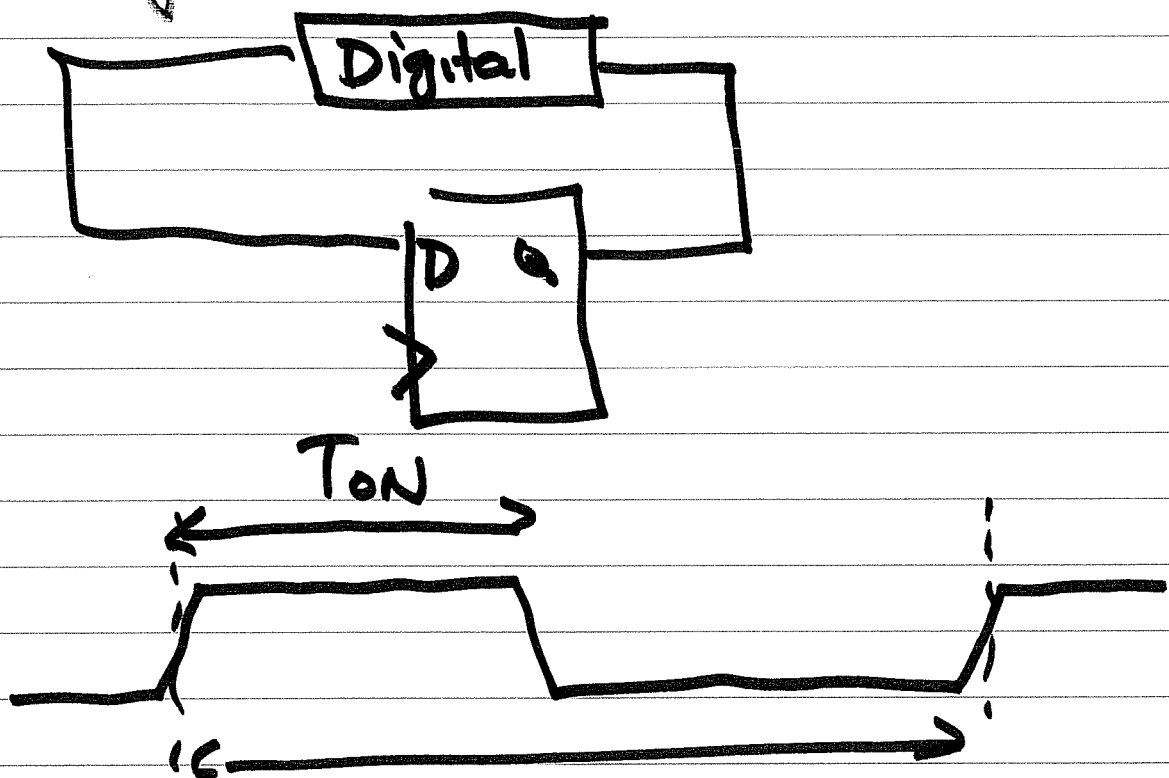


Sequential Machines

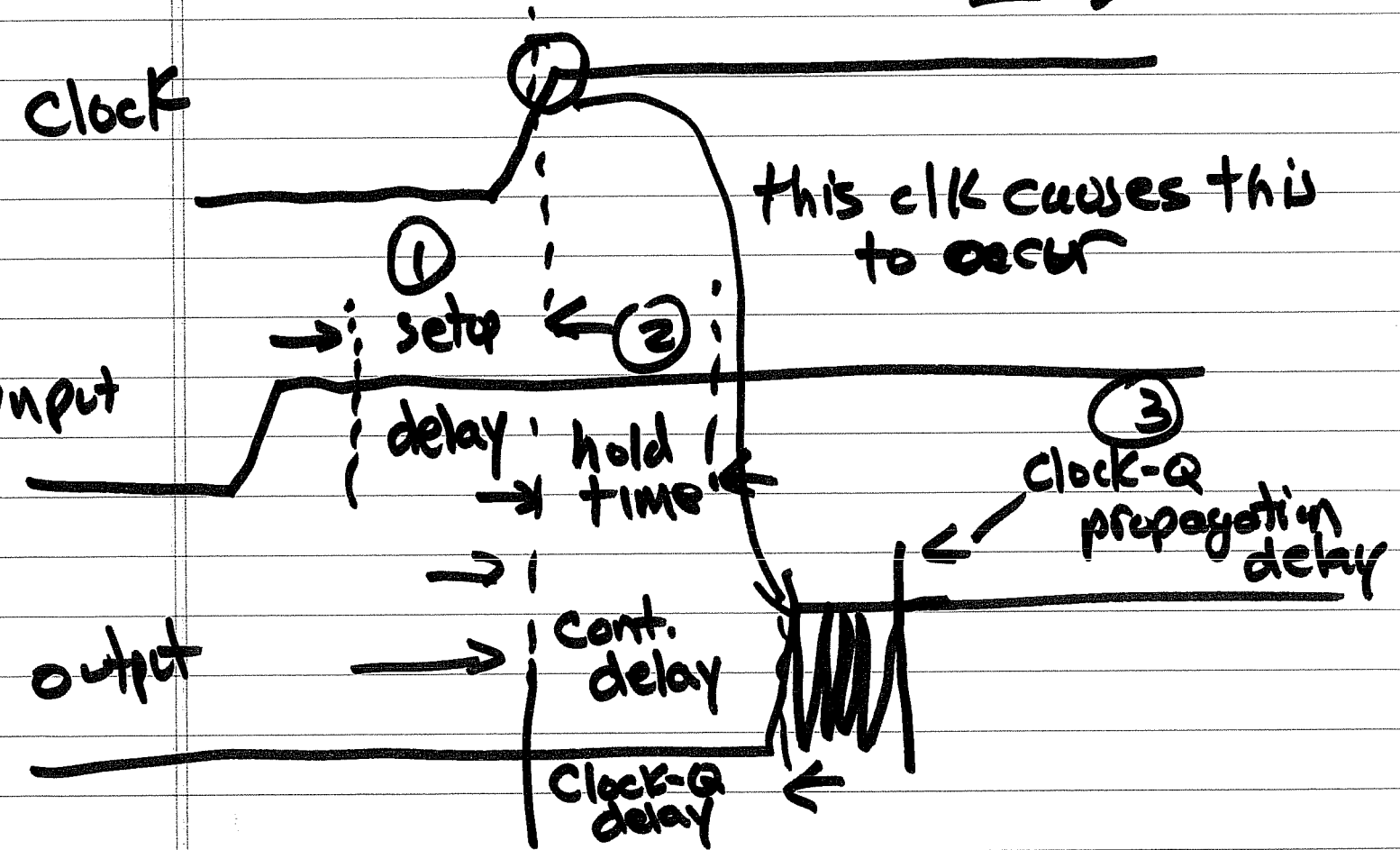
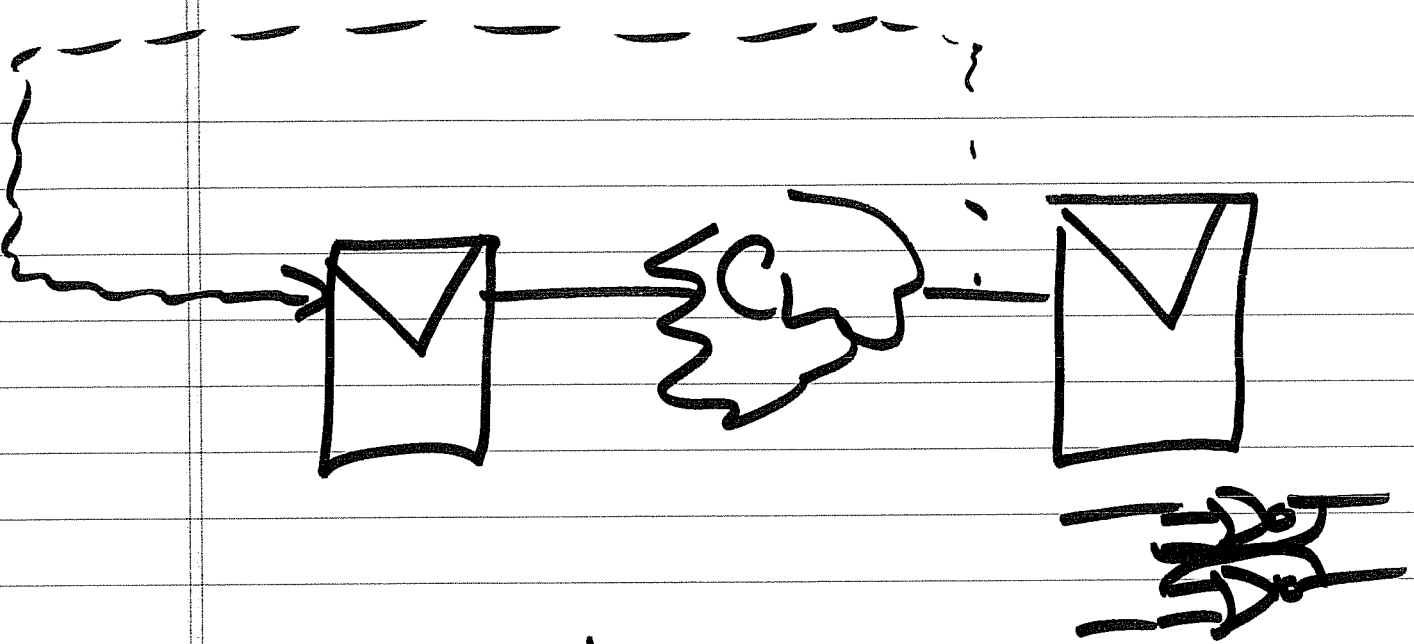


$T_c = \text{cycle time}$

$f_c = 1 \text{ GHz}$ Pentium processor

$$T_c = \frac{1}{f_c} = \frac{1}{1 \times 10^9 \text{ Hz}} = 1 \times 10^{-9} \text{ sec} = 1 \text{ nsec}$$

$$\text{Duty cycle} = \frac{T_{ON}}{T_c} = 50\%$$



Setup time = min time before clock edge, that the input must be available

hold = same as setup but min time after clock

$$T_c \geq t_{pcq} + t_{pcl} + t_{setup}$$

clock
Q time

prop
delay
of
Comb.
logic

forbidden
zone

max-delay
constraints

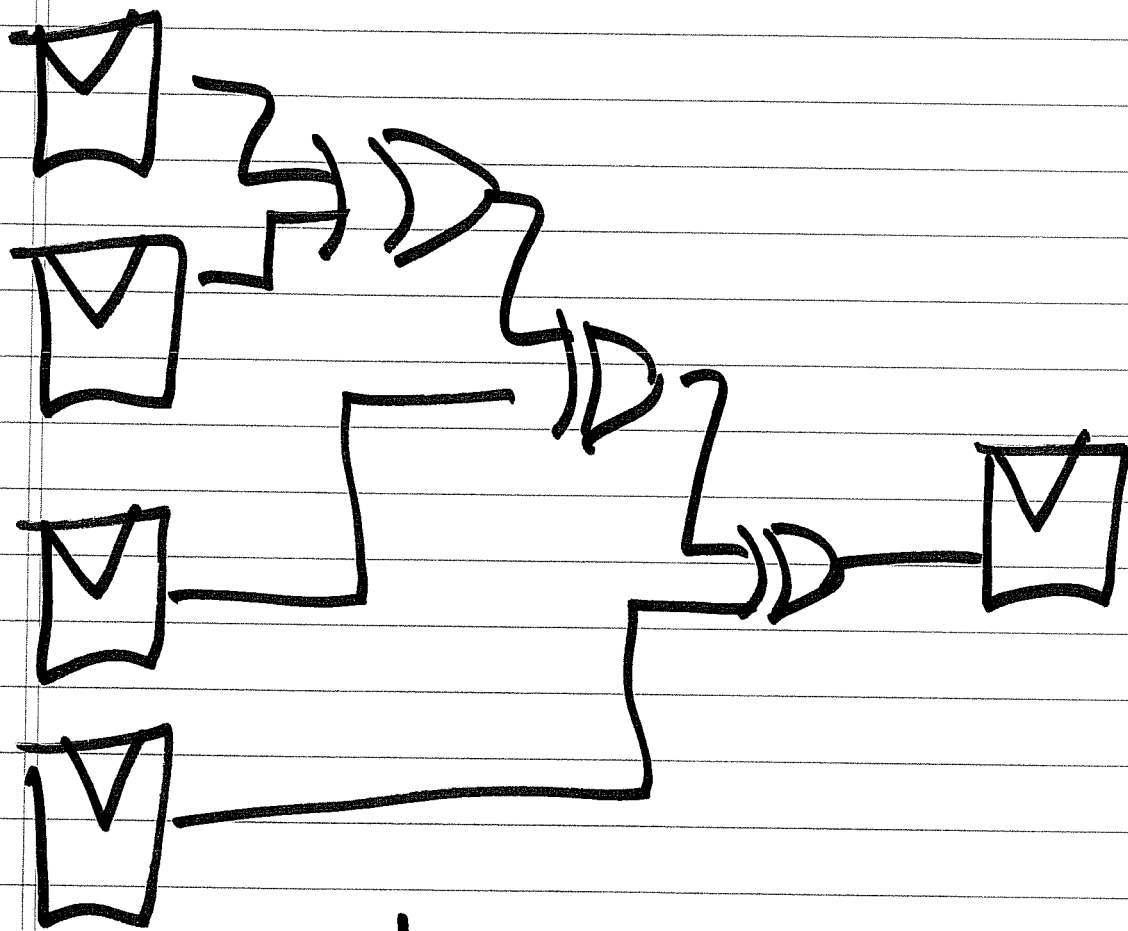
(critical path)

$$t_{pcl} \leq T_c - (t_{pcq} + t_{setup})$$

Sequencing
overhead

min delay
constraints

$$t_{ccL} + t_{ccQ} \geq t_{hold}$$



$$t_{pxor} = 100ps$$

$$t_{cxor} = 55ps$$

$$t_{FFsetup} = 60ps$$

$$t_{FFhold} = 20ps$$

$$t_{paccq} = 70ps$$

$$t_{ccq} = 50ps$$

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$$T_c \geq t_{pcq} + t_{pcl} + t_{setup}$$

$$\geq 70 \text{ ps} + 3(100) + 60$$

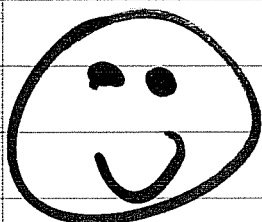
$$\geq 430 \text{ ps} \quad \text{Max delay constraint.}$$

$$f_c = \frac{1}{T_c} = 2.33 \text{ GHz}$$

$$t_{ccq} + t_{ecL} > t_{hold}$$

$$50 + 55 > 20 \text{ ps}$$

$$105 \text{ ps} > 20 \text{ ps}$$



Min delay constraints