

# Announcements

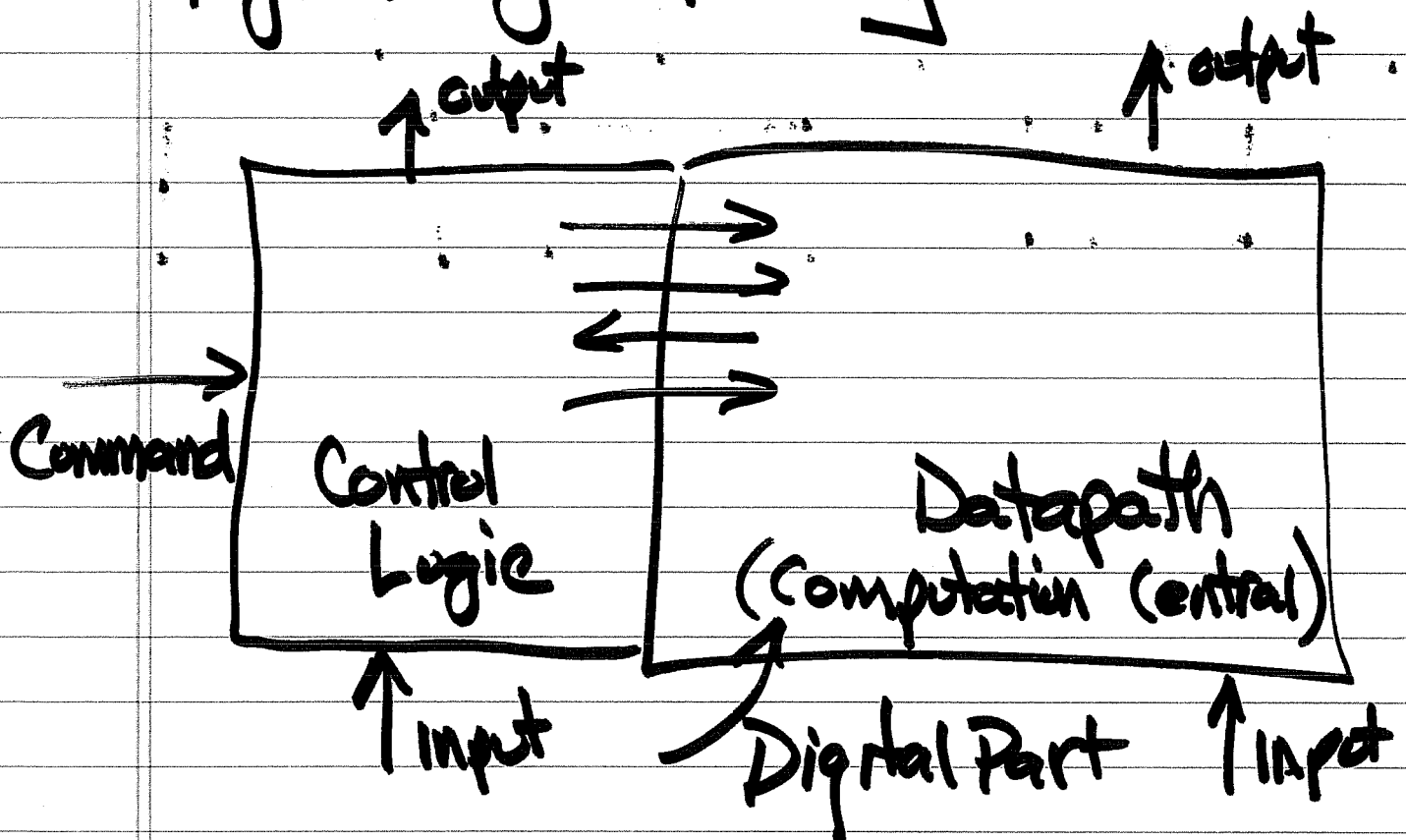
test next week - up to Chapter 4

Project

April 24 - ARM 10:30-11:20AM

↳ ARM / Thumb

# Digital System Design



# MIPS R2000

www.mips.com

Stanford

John Hennessy

David Patterson

MIPS R4000

Nintendo 64

## Commands

LW

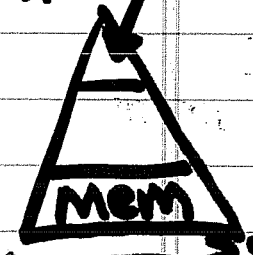
load  
word

RTL

$$Z[RD] = \text{Mem} \\ \uparrow \\ RF$$

Mnemonics

FAST RF



Cheat: loads value from memory into register file

[ ] = contents of RF

Add

Adds 2 values from RF into RF

$$Z[RD] = A[RS] + B[RT]$$

Addi

Adds 1 value  
from RF and  
a const and  
puts back into  
RF

$$Z[RD] = A[RS] + \{2'b00, \text{const}\}$$

$$\{2'b10, 3'h7\} = 10111$$

↑ concatenation

5 bits

$$\{3 \{2'b10, 3'h7\}\} = 1011101110111$$

↑ repetition

SW

Stores value  
into memory  
from RF

$$\text{Mem} = Z[RD]$$

Why can't I have an instruction  
that  $\text{Mem} = A[RS] + B[RT]$

Make common case fast!

4-bits

Dual Ported

