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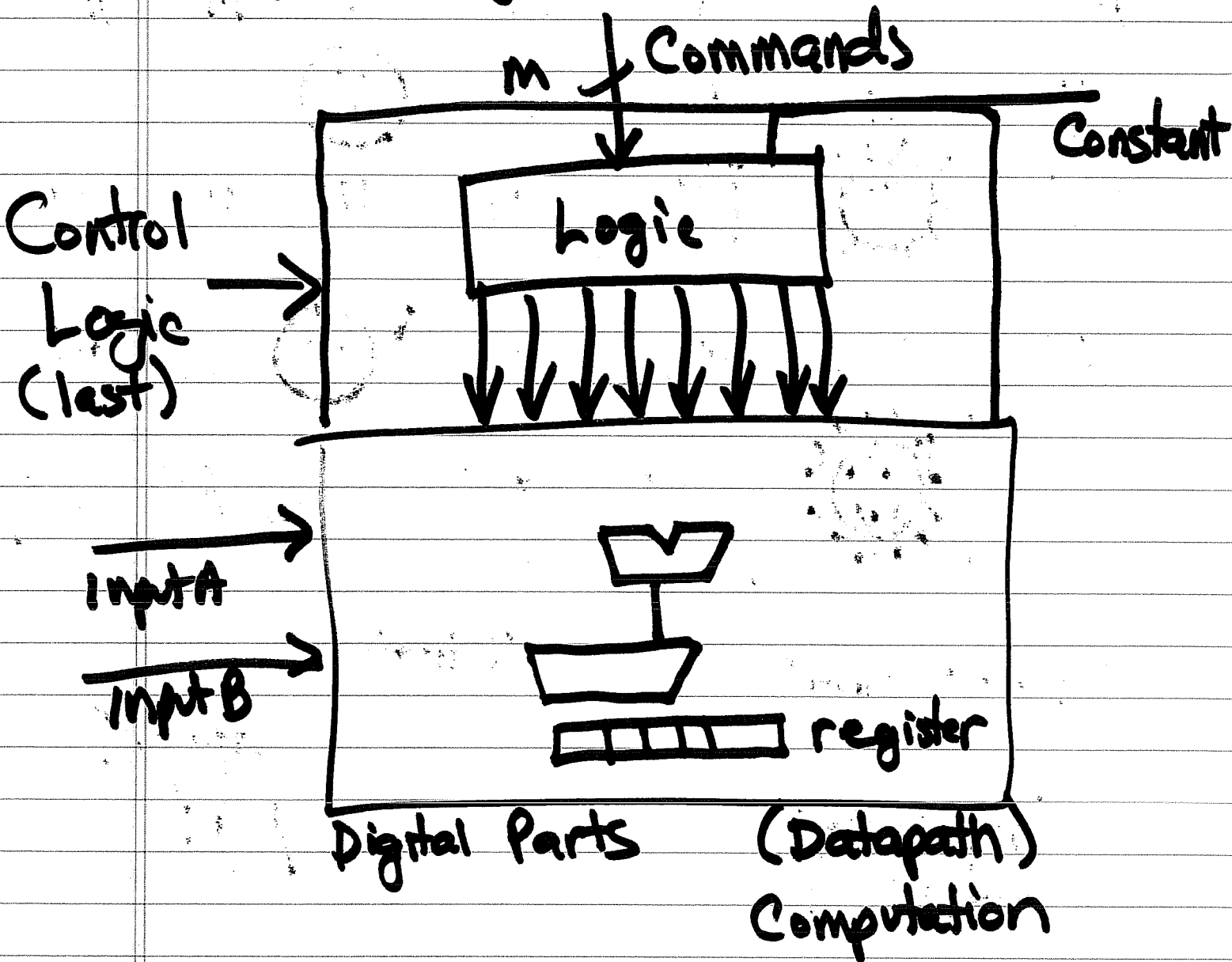
Design Day

test 2

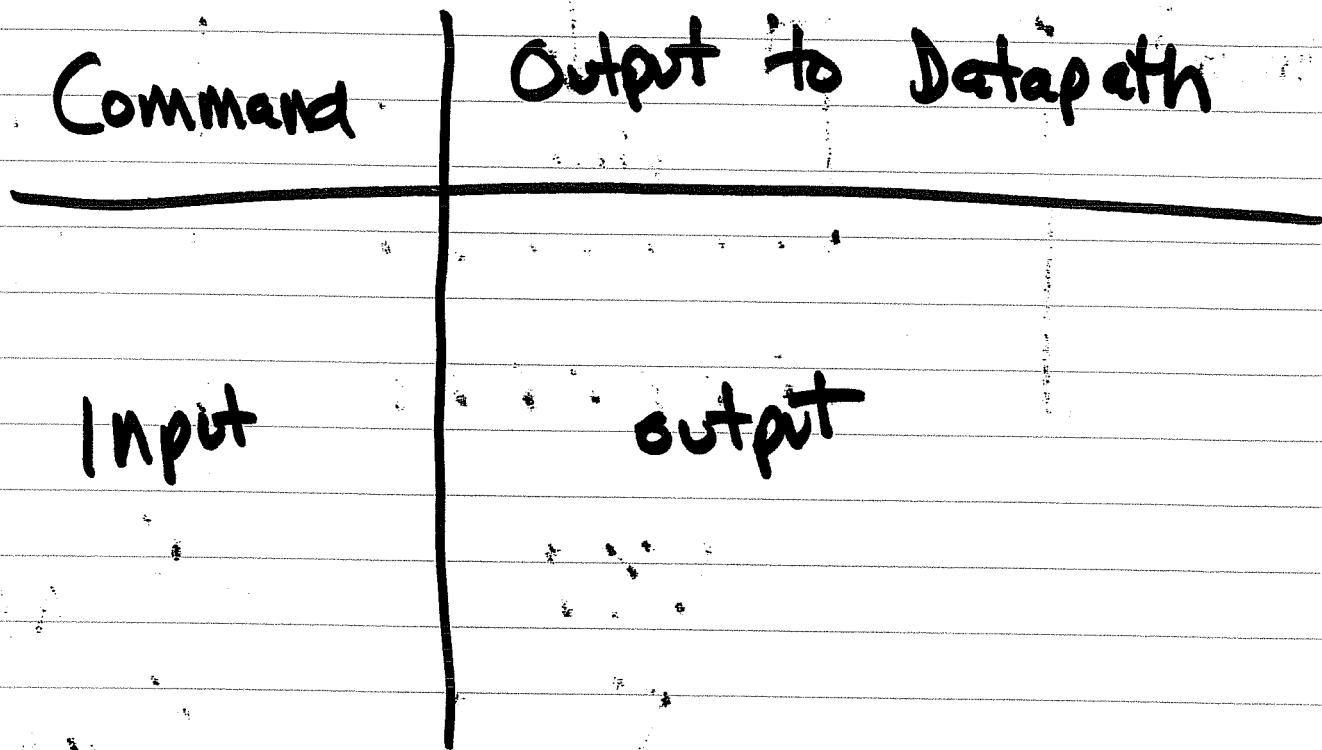
Dead Week

LAB Report (if ! poster)

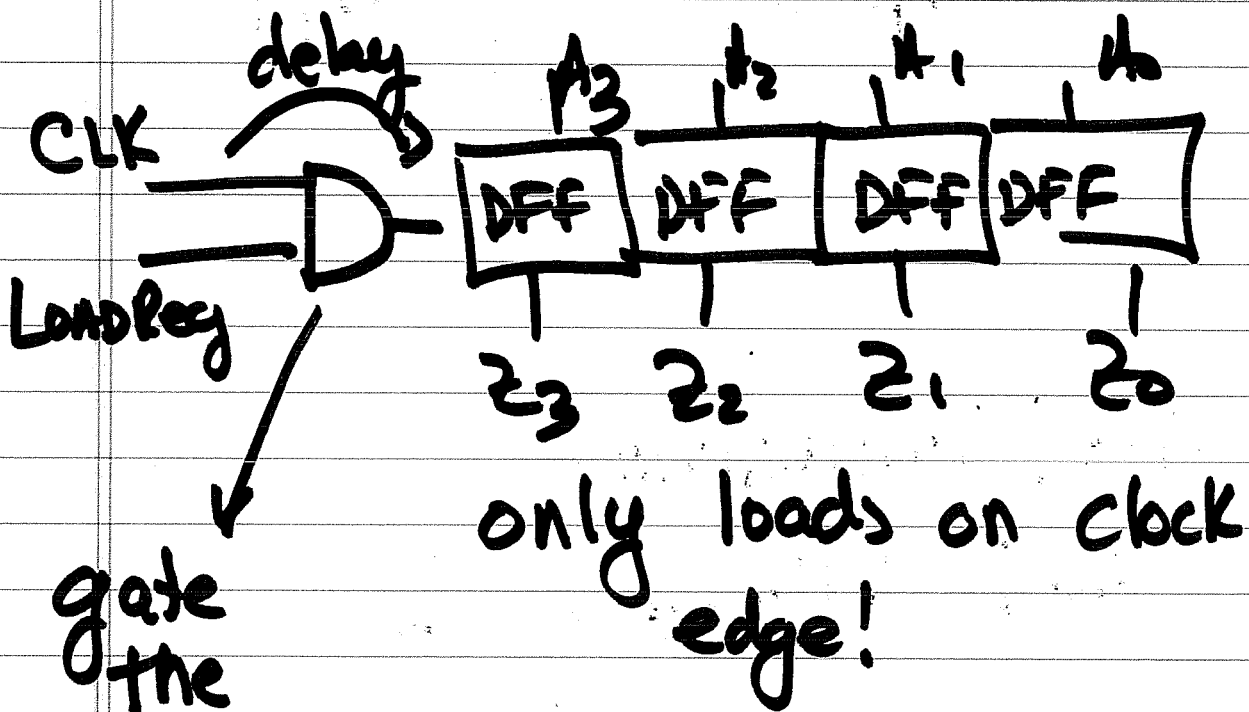
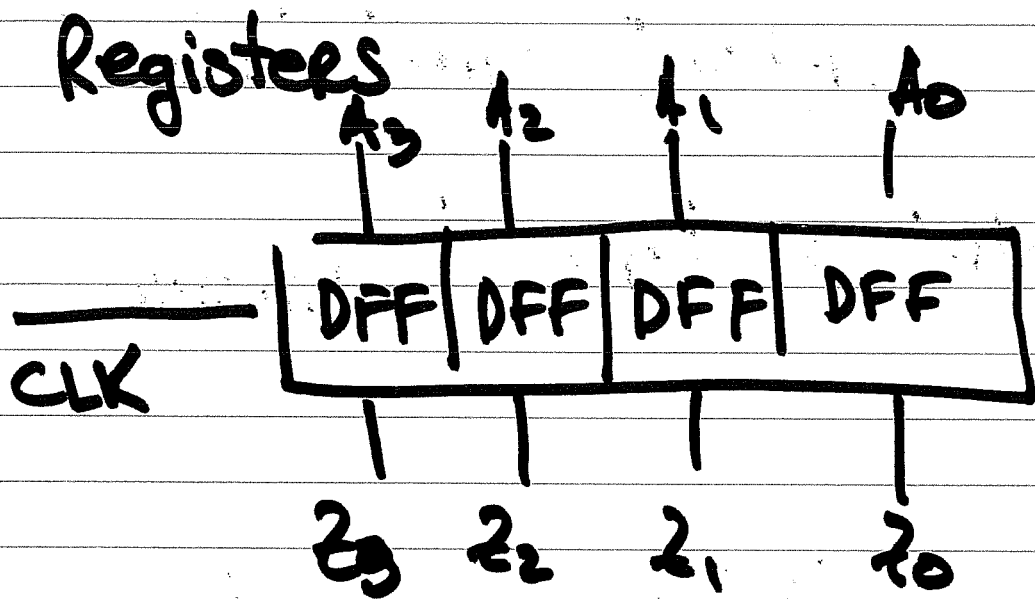
# Digital System Design



# Control Logic Design



- 1.) Combinational Logic
- 2.) Sequential Logic
- 3.) Memory (PC)



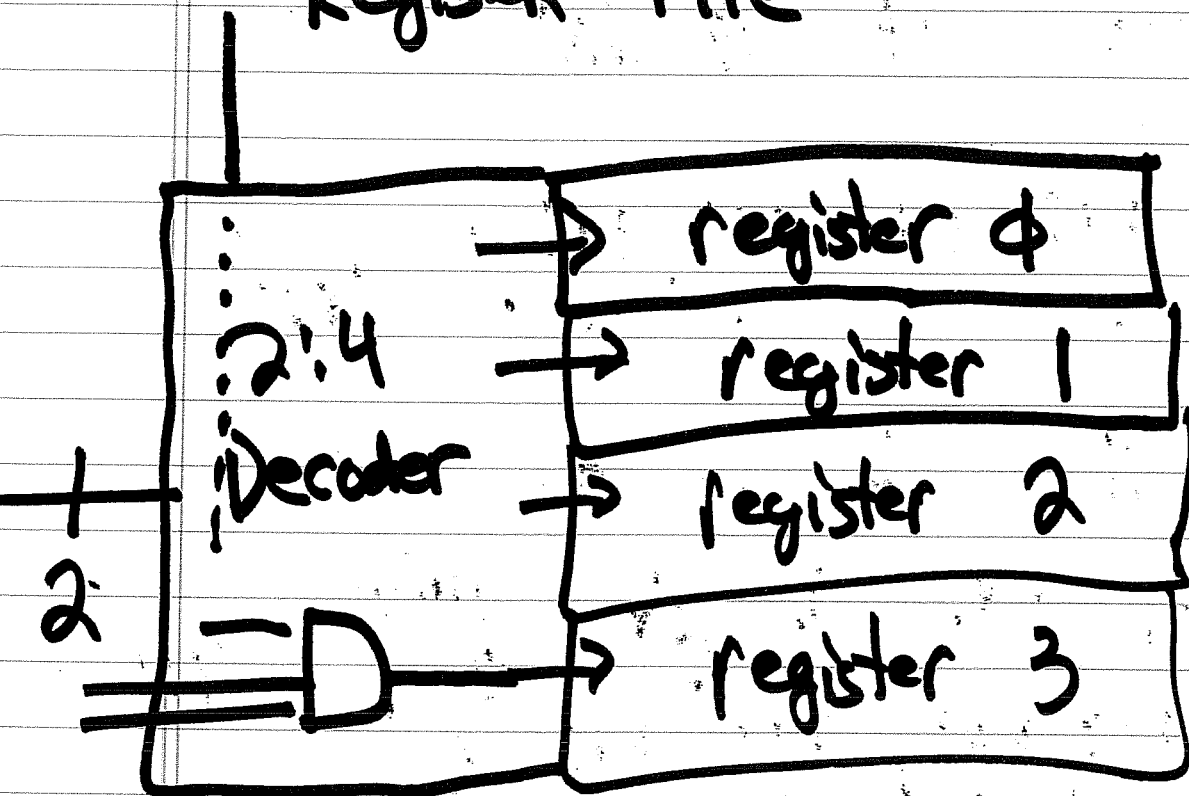
gate the clock

Adv: load any time

Dis: incurs delay (skew)

gating the clock causes skew

# Register File



Register file is composed of more than 1 register to store and read data