

Full Name: _____

Digital Logic Design, Spring 2008

Exam 2

April 17, 2008

Instructions:

- Make sure that your exam is not missing any sheets, then write your full name on the front.
- Write your answers in the space provided below the problem. If you make a mess, clearly indicate your final answer.
- The exam has a maximum score of 100 points.
- The problems are of varying difficulty. The point value of each problem is indicated. Pile up the easy points quickly and then come back to the harder problems.
- This exam is CLOSED BOOK. You are only allowed to use the single sheet of notes you made for this exam. Please hand in this sheet along with your test. Good luck!
- Each extra credit is only worth 1 point.

1 (10):
2 (10):
3 (20):
4 (20):
5 (40):
TOTAL (100):

Problem 1. (10 points):

What is the difference between a latch and a flip-flop? Under what circumstances is each one preferable?

Problem 2. (10 points):

Design a 2-bit counter finite state machine.

Problem 3. (20 points):

What is a tristate buffer? How and why is it used?

Problem 4. (20 points):

Show a schematic for the following Boolean equation. Assuming each gate takes the same delay, show the worst-case or critical-path delay.

$$F = \overline{\overline{(A \cdot B)} \cdot \overline{(C \cdot D)}} \cdot E$$

Problem 5. (40 points):

You are designing an elevator controller for a building with 25 floors. The controller has two inputs: UP and DOWN. It produces an output indicating the floor taht the elevator is on. There is no floor 13, which is still a common architecture design technique. What is the minimum number of bits of state in the controller?

Problem 6. (40 points):

For problem 4, write the Verilog for this design.

Problem 7. (40 points):

Write an HDL module that computes a five-input XOR function assuming the input is $a_{4:0}$ and the output is y .

Problem 8. (40 points):

Design a structural Verilog HDL module for a 16 : 1 multiplexor. This device selects between 16 inputs and produces an output based on a select signal.

Problem 9. (40 points):

Write a line of HDL code that gates a 32-bit bus called *data* with another signal called *sel* to produce a 32-bit result. If *sel* is TRUE, then *result* = *data*. Otherwise, *result* should be all 0s.

Problem 10. (40 points):

Design a 5-bit ripple-carry adder.

Problem 11. (40 points):

Design a 4-bit left and right rotators. Sketch a schematic of your design and implement in the Verilog HDL.

Problem 12. (40 points):

Design a shifter that always shifts a 32-bit input left by 2 bits. The input and output are both 32 bits. Explain the design in words and sketch a schematic. Implement your design using a behavior and structural Verilog HDL.

Problem 13. (40 points):

What are the advantages and disadvantages of structural vs. behavior HDL design?

Problem 14. (40 points):

An incrementor adds 1 to an N -bit number. Build an 8-bit incrementer using half adders.

Problem 15. (40 points):

Suppose a designer was creating a design provided 1 input operand of 4-bits and the following commands:

- command 1: Output = input
- command 2: Output = 3
- command 3: Output = input + 2
- command 4: Output = 0

Design this digital logic using an appropriate methodology. It is best to give this design as a schematic and not a Verilog HDL.

Problem 16. (40 points):

Design a Finite State Machine that asserts the output Q when A AND B are **TRUE**.

Problem 17. (40 points):

Design a Finite State Machine that asserts the output Q for one clock if A is TRUE followed by B being TRUE during the next cycle.