

## Laboratory Syllabus

The following syllabus explains the expectations and setup of the laboratory for the Spring 2008 semester.

**Introduction and Procedure:** The laboratory component of this course introduces and reinforces important aspects of digital logic. Your lab will meet once each week, where you will complete approximately seven laboratory assignments during the course of the semester. Approximately the first six projects will serve to introduce you to various concepts and design techniques. All but two labs will involve teamwork. The last project will be a significant team oriented design exercise that will last about half the semester.

You should be enrolled in one of the lab sections. Please come to lab during the section for which you are enrolled – it is sometimes acceptable to come to a different session if an unforeseen conflict arises, but you should clear this with the lab TA ahead of time as labs are limited to no more than 14 students. Any permanent change in lab section should be accomplished by enrolling in the new section.

The first few labs will have a relatively rigid structure. When you begin team oriented lab assignments, you will be given more freedom in scheduling your lab time. Each laboratory assignment will typically consist of three parts:

- Pre-lab proposal,
- Laboratory experiment (to be completed in lab), and
- Post-lab documentation.

Failure to reasonably complete any portion of the lab assignment will result in a 50% penalty on the lab.

**Proposal:** The pre-lab proposal portion of the assignment is to be completed individually (except during team assignments) outside of lab and turned in to your lab instructor (TA) for approval at the **beginning** of your laboratory session the following week. The pre-lab proposal is intended to prepare you for the in-lab portion of the assignment and may be quite involved, so it's important that you allocate sufficient time to complete it prior to coming to your lab session. After the TA has received and initialed your pre-lab, you will be allowed to proceed with the in-lab portion of the assignment.

Pre-lab assignments may sometimes require you to construct a circuit prior to coming to lab. Each lab assignment will contain specific instructions. Failure to complete a pre-lab assignment will result in a 50% penalty on the lab.

***In-Lab Procedure:*** In-lab work is completed either individually or in pre-assigned teams of students. The early lab assignments are individual so that everyone will have an adequate chance to learn the basics of prototyping and circuit design. Teamwork will start with the third lab assignment. When working as part of a team, all students should stay involved in order to learn and understand the principles. This will help ensure that you are prepared for the lab practical exam to be completed independently by each student later in the semester. Peer evaluation will be used to gauge individual participation. Be sure to carry your own weight as peer evaluation will affect your final grade.

***Post-Lab Documentation:*** After completing the in-lab portion of the exercise, you must complete a short report describing your design, the procedures you followed, and addressing any specific questions posed in the assignment. This comprises your post lab documentation. The post-lab report is completed outside of lab and will be due at the beginning of your lab session the week following the in-lab exercise. You will also have a pre-lab proposal for the next lab due at the same time. A sample post-lab report will be made available on the web site for you to use in preparing your own reports. Team assignments require only one post-lab document from your group.

***Missed Labs:*** In general, missed labs may not be made up. However, there may be circumstances where you can make up a missed lab the same week by attending another lab section. Check with your lab TA to make arrangements.

***Lab Practical Exam:*** Approximately mid-way through the semester, a lab practical exam covering the skills and principles you learned in lab will be administered to each student. It must be taken, at the assigned time, in order to pass the course. The lab practical exam is worth 10% of your total lab grade.

***Lab Instructor:*** There are two TAs for the course. The TA should be your first resource when you have questions relating to the lab or classroom assignments. The TAs are responsible for both lab instruction and grading of all assignments. Your TA may be contacted either by email or in person during one of the scheduled lab sessions. If you choose to contact the TA during a scheduled lab session, wait until he isn't busy with another student. Homework and lab questions may be referred to the instructor if the TA is unavailable to help you first.

**Harsha Choday**  
harsha.choday@okstate.edu

**Jun Chen**  
jun.chen@okstate.edu

***Parts Kits:*** Three kits of parts will be available. (1) integrated circuit logic elements, (2) an FPGA evaluation module, and (3) a Protoboard. The first kit consists of the electronic

components you will need for the early labs. It will be supplied to you during your first lab. The second kit consists of a Xilinx Spartan3E FPGA from Digilent and jumper cables that you will need in order to build more complex circuitry. It will be supplied to you during your second lab. The third kit is optional and includes a protoboard and stripped hookup wire. If you are enrolled in one of the methods labs (ECEN 2011, ECEN 3714 or ECEN 3314) then you already have a wire kit and protoboard. If not, a protoboard and wire kit can be purchased (in ES 101) at any time during the semester. Your bursar account will automatically be billed for the first two lab kits. **Lab kits may not be returned.** Your two required lab kit will cost approximately \$170.00. The optional protoboard and wire kit are approximately \$16.00 and \$8.00, respectively.

As you progress through the lab exercises you may find that you need or want parts that are not in your parts kit. Most common parts can be purchased in ES 101 at a small cost. One of the objectives of this lab is to have you make design decisions that include choosing the method of solution (and the parts) for your design. The TAs will provide assistance as needed.

**Course Notes:** Copies of lecture slides, lab assignments, various handouts and last-minute announcements will be posted on the class web site. Please check it regularly.

**Software:** The student edition of *XILINX ISE 9.2i* is available on the *XILINX* Website, allowing you to install it at home if you desire. This software will be used for many of the laboratory assignments dealing with programmable logic devices. Installation and usage help can be found on the class web site and at the *XILINX* Website. This software package is available in the CEAT PC labs and in the digital logic lab (ES 301). The TAs can provide assistance.

**Lab Computers:** The laboratory computers will be used to construct schematics, state diagrams, and program the FPGAs using *XILINX*. They are also equipped with Microsoft Office 2003 and browsing software. Only students enrolled in the class may use the lab computers. To ensure this and that your data is not reused or falsified, you will be given a team login, password, and space for data storage. Though your data can be stored onto your team's allotted server space, you should not rely on it. The server could lose data for any number of reasons. Because of this, you should back up all data you do during lab onto a personal flash memory stick or CD-R.

**Grading:** Your lab grade will be factored into your overall class grade as described in the class syllabus. Your labs will be graded on achievement, content, and appearance. Neatness and organization are both important – excessive messiness will result in lost points. Be sure to follow the instructions given in lab.

***Getting Assistance:*** If time permits we will schedule a help session once each week (time to be announced) where a TA can answer your questions. You may also ask for assistance from the TAs during regularly scheduled lab sessions. The class web site contains documents and links that you may find helpful. In addition, the honor society for electrical and computer engineering, Eta Kappa Nu (HKN), has also volunteered their time, offering help sessions for many ECEN courses twice weekly (that includes this course). HKN will announce these times at the beginning of the semester during class.

***Academic Dishonesty/Misconduct:*** As an Electrical Engineering student at Oklahoma State University, you are expected to uphold the highest standard of academic honesty. *Cheating on exams or quizzes, plagiarism, and copying of labs or homework will not be tolerated.* Discussion of assignments with other students for the purpose of learning the material is encouraged; however, you should always complete your pre-labs, post labs and other assignments as instructed (independently unless otherwise indicated) – the work you turn in should always be your own. Violations will be handled in compliance with the guidelines established by the Office of Student Conduct. The instructor will give a maximum penalty of an "F" course grade in such situations.

***Disability:*** If any member of the class feels that he/she has a disability and needs special accommodations of any nature whatsoever, I will work with you and the University Office of Disabled Student Services (326 Student Union) to provide reasonable accommodations to ensure that you have a fair opportunity to perform in this class. Please advise me of any such disability and the desired accommodations at the earliest possible time -- on the first day of class if possible.