

## **CAD Tool Hints**

*Digital Design and Computer Architecture*, Harris and Harris, © Elsevier, 2007

### **Xilinx ISE 9.2i, ModelSim 6.2g, SPIM**

## **Introduction**

The following three sections describe Xilinx ISE, ModelSim, and SPIM. Each of three sections has two parts: an overview and a list of helpful hints.

### **Xilinx ISE 9.2i (Project Navigator)**

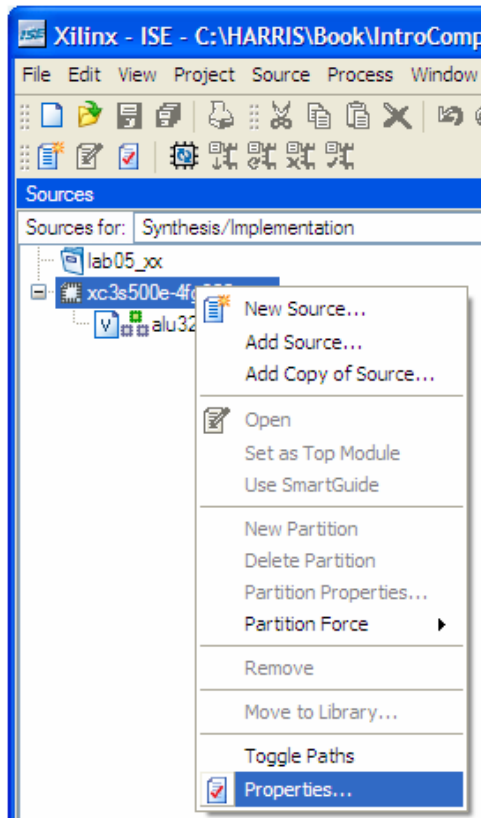
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#### **Overview:**

- Xilinx Project Navigator allows users to enter digital designs as either schematics or HDL modules.

#### **Helpful Hints:**

- Make sure you don't have any spaces in the path to any of your Xilinx directories or Xilinx will complain. (Or worse, Xilinx might not complain and instead die a slow, silent death.) For example, the Desktop has spaces in the path (e.g., C:\Documents and Settings\Administrator\Desktop).
- Sometimes it looks as if wires in the schematic disappear. You likely simply need to refresh the screen by pressing the F5 key.
- Warning: after saving a schematic or HDL file, the "undo" command no longer works.
- You can change the properties of a project at any time by right-clicking on the high level project in the Sources pane and selecting Properties, as shown below.




- To select the size of a schematic, right-click on any empty part of the schematic and select “Object Properties”. Select the desired paper size from the scroll down menu of “Schematic Properties” and click “OK”. It will then give you a warning that this operation cannot be undone and ask if you want to continue. Click “Yes”.
- Make sure you don’t have any spaces in the path to any of your Xilinx directories or Xilinx will complain.
- When you connect two wires together, Xilinx names them the same thing. If you later decide to disconnect two wires that were previously connected, you need to delete at least one of the nets completely and replace it. If you **don’t** do this, Xilinx will continue trying to name them the same thing and think they are connected.
- To erase just part of a wire (not the entire branch), choose “Select the line segment” instead of “select the entire branch” under the Select Options.
- If you have difficulty routing a wire, try manually routing it by clicking on “Use the Manual method...” under “Add Wire”. You might also try zooming into the area where you want to place it and then try routing it again (either Autoroute or Manual).
- If the incorrect inputs and output ports show up when you try to assign your package pins, open the verilog file “lab02\_xx.vf” using your favorite text editor or by opening it in Xilinx using File→Open. Move the top-level module, the module

that has the inputs D(3:0) and outputs S(6:0), to the top of the file. The top-level module begins with the key words “module lab02\_xx” and ends with the key words “endmodule”. Move this entire module to the top of the .vf file, directly below the following lines:

```
// This verilog netlist is translated from an ECS schematic. It can be
// synthesized and simulated, but it should not be modified.
//
`timescale 1ns / 1ps
```

Be sure to copy and paste the entire module. Save the verilog file and try assigning the package pins again.

- If there’s a red dot at the end of a wire, the wire is not connected to anything. Sometimes it may look like the wire is attached to the input of a logic gate, but the dark dot is the giveaway that there is no connection. Delete the wire and try redrawing it. Often this bug and the next one will manifest themselves as gray boxes somewhere in your simulation indicating floating outputs.:
- Remember, if you want to delete just part of a wire (not all of its connections – i.e. the “branch”), click on “Select the line segment” under the “When you click on a branch” section in the Select Options window on the left-hand side of your schematic window.
- If you place two gates nearby so that the output of one touches the input of another, make sure the gates connect. You can drag gates around to see if they are really connected.
- When you see warning messages in the Project Navigator window, pay heed to them, especially when your circuit isn’t working. Understand what warnings are normal and what ones indicate a problem.
- If you make a change in your schematic, sometimes the simulator will not know about it. The best thing to do is quit the simulator and restart it.
- If everything seems right and the tools are still acting up, try quitting and restarting Project Navigator. If you constantly see the same error message when you check the errors of your schematic, try to exit the editor and re-enter and see if the error message is gone. Sometimes, the editor is not properly updated about the corrections you have done.
- In creating the symbol out of your schematic, if you want to rearrange the pin layout of the symbol, make sure always move the name with the end connection together so you don’t scramble them logically. (**THIS IS VERY IMPORTANT**)
- Be careful, if you draw a wire across a pin, Xilinx may connect to the pin without your intending to.
- Before doing simulation, always check your schematic files. Correct all the errors.

- You can save the format of your testbench waveform outputs (i.e. the order and format of your inputs and outputs in Modelsim) by doing the following. After opening your testbench waveform in Modelsim and ordering the inputs and outputs as you would like, choose **File->Save**, or by clicking on the Save icon . Save the format file with a “.do” suffix. Make sure the “wave-default” pane is selected.

Next time you make changes to your schematic or waveform, you can open the saved format in the waveform viewer in Modelsim. First, make sure the “wave-default” pane is selected. Then (1) choose Edit->Select All and Edit->Delete to delete the current signals and (2) choose File->Load and open the file you previously saved “.do” file.

- If you make a change in a lower-level schematic, remember that you must create the symbol again for that schematic and then update it in the higher-level schematic. Once you have successfully created a schematic symbol for a schematic, you will see a green check mark by the Create Schematic Symbols option in the Processes window when you highlight the given schematic in the Sources window.
- Timing constraints for testbench waveforms can be changed in the HDL Bencher window by selecting **Test Bench → Rescale Timing** from the file menu.
- You can also change the simulation end time in one of two ways: (1) Double-click the upper left-hand text called “End Time” in the Testbench Waveform panel and enter a value. (2) You can select **Testbench→Set End of Test Bench** from the file menu and type the desired value in the end time box. (Theoretically, you should also be able to do this by typing the value end time box at the top of the panel that defaults to 1000 ns. However, this interface seems to be buggy.)
- To synthesize a module, it must be selected as the “top module” in Xilinx Project Navigator. To do so, right-click on the module you’d like to synthesize in the Processes pane in Project navigator and select “Set as Top Module” in the pull-down menu. Alternatively, you can synthesize the higher-level modules, which will, in turn, synthesize all of its lower-level components. The RTL and technology schematics of the lower-level modules can be viewed by double-clicking on the higher-level modules until the lower-level schematic is reached.

## **ModelSim Xilinx Edition-III (MXE-III) 6.2g**

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### **Overview:**

- ModelSim is a digital circuit simulator. After entering a design in Xilinx Project Navigator, ModelSim can be invoked from within Project Navigator to simulate the circuit.

## Helpful Hints:

- You can choose hexadecimal as the default radix by choosing Simulate → Runtime Options in the ModelSim toolbar. In the pop-up window choose Hexadecimal as the default radix
- MXE-III is a limited edition of ModelSim and will only let you run a simulation for at most 1000 ns.
- In ModelSim, you can view signals internal to your Verilog module (i.e. signals that are not inputs or outputs to the module). To do so, begin by running your testbench on ModelSim. View the “Workspace” window in the main ModelSim window. Expand the hierarchy of the modules until you find the unit under test (UUT), your FSM module. Double-click on the UUT, as shown below in Figure 3, to display all the signals associated with that module in the Objects window next to it. (You may need to expand the Objects window to view the signals.)

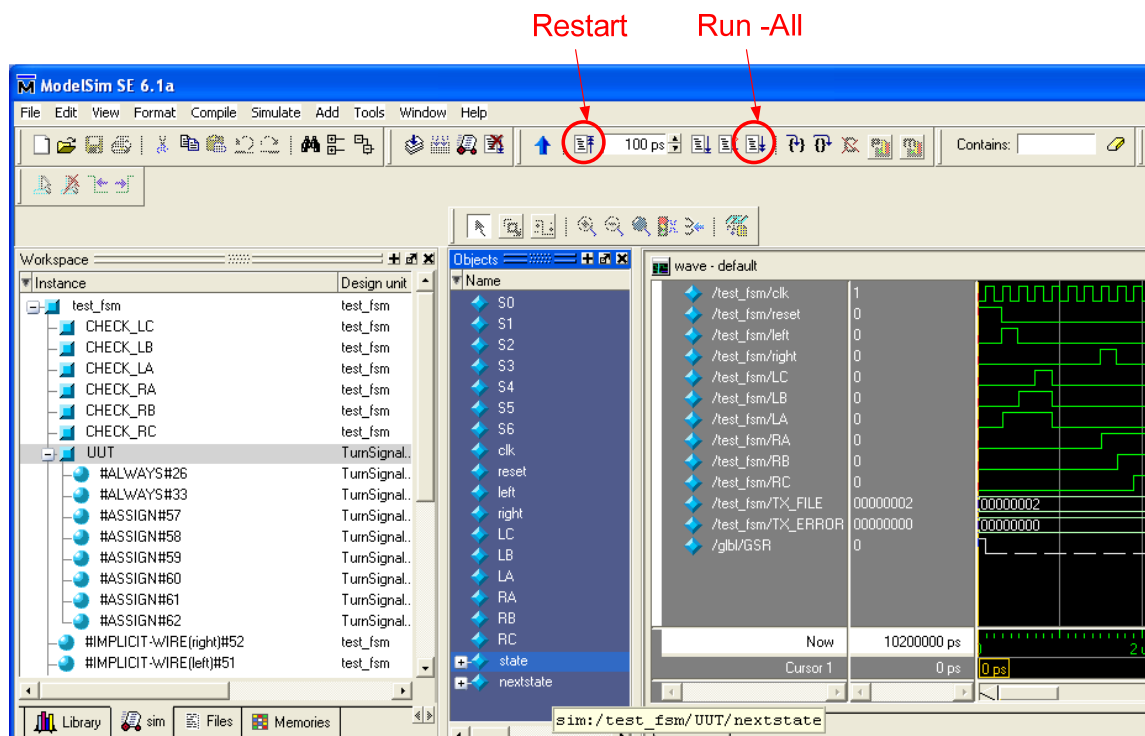




Figure 3

Click on the signal you would like to view in the waveform window and drag it to the waves window (labeled “wave-default”). For example, you might want to view the state signal. After you have dragged the signals you would like to view to the waves window, you will need to resimulate. Again in the main ModelSim window, click on Restart , and then Run-All , as shown in Figure 3 above. You can change the amount of time it runs for by changing the time in the box to the left of the Run-all symbol (currently at 100 ps).

During debug, you'll likely want to view several internal signals. However, on the final waveform that you turn in, make sure to display only the required signals in the correct order. All the signals must be readable to get full credit.

- You can save the signals displayed in the Modelsim waveform by choosing File→Save. It will list “wave.do” as the default filename. You can use that filename or rename it to another .do filename. After exiting and reopening Modelsim, you can reload the signals you saved in the .do file. First delete all of the current signals shown in the waveform by choosing Edit→Select All. Then press the Delete key. The waveform should now show no signals. Then choose File->Load and reload the .do file. You will need to Restart and Run-All to view the signal values.

## **SPIM, a MIPS Simulator**

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### **Overview:**

- SPIM is a MIPS simulator. A user writes an assembly program in a text editor and can then open and run the program using SPIM. SPIM shows the machine instructions of the program and the state of the registers and memory.

### **Helpful Hints:**

- Make sure the exception handler is correctly referenced. SPIM will prompt you if it cannot find it.