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# Digital Logic Design

## ECEN 3233

### Module 11 – CPLD and FPGA

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Weihua Sheng  
School of Electrical and Computer Engineering  
Oklahoma State University

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and Randy H. Katz

1

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## Programmable Logic Arrays (PLAs)

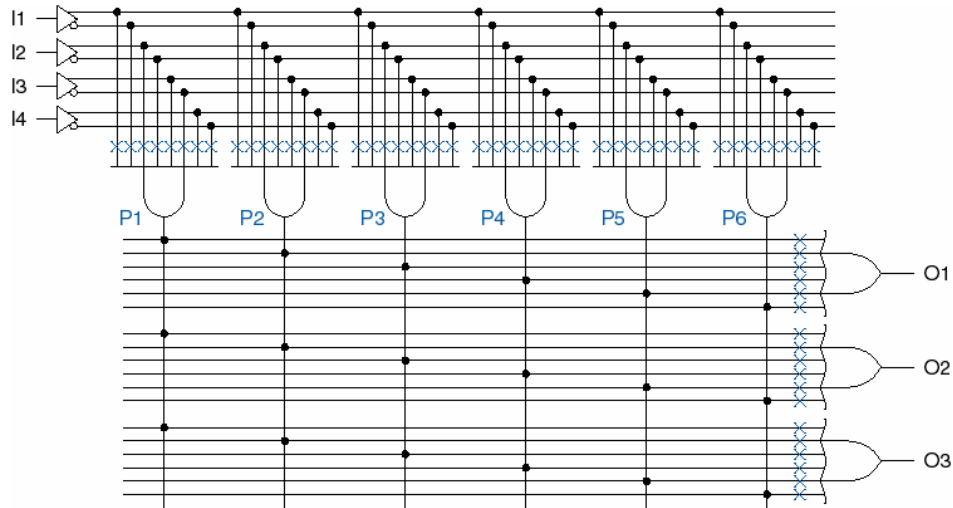
### **Recall:**

- Any combinational logic function can be realized as a sum of products.
- Idea: Build a large AND-OR array with lots of inputs and product terms, and programmable connections.
  - $n$  inputs
    - AND gates have  $2n$  inputs -- true and complement of each variable.
  - $m$  outputs, driven by large OR gates
    - Each AND gate is programmably connected to each output's OR gate.
  - $p$  AND gates ( $p \ll 2^n$ )

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2

## Example: 4x3 PLA, 6 product terms

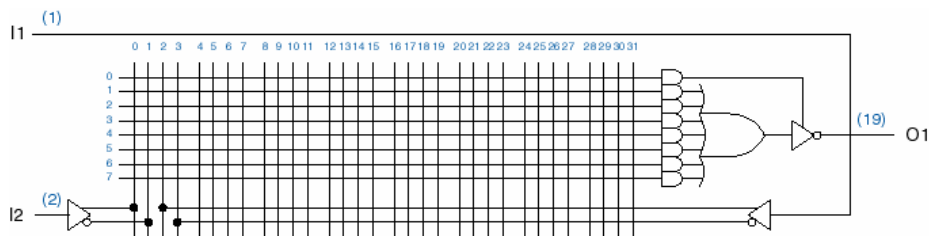


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3

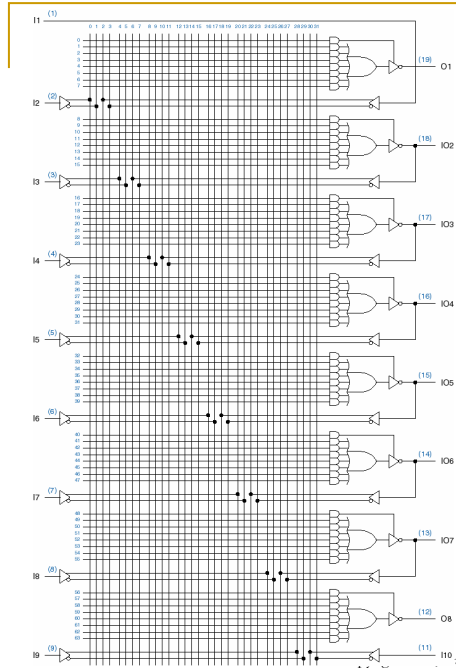
## Programmable Array Logic (PALs)

- PALs ==> *fixed* OR array
  - Each AND gate is permanently connected to a certain OR gate.
- Example: PAL16L8 (below and next slide)



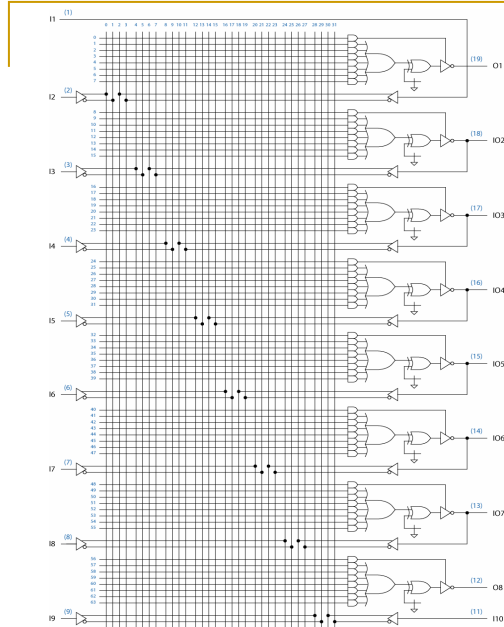
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4



- PAL16L8
  - 16 total inputs
  - 8 total outputs
- 10 primary inputs
- 8 outputs, with 7 ANDs per output
- 1 AND for 3-state enable
- 6 outputs available as inputs
  - more inputs, at expense of outputs
- Note inversion on outputs
  - output is complement of sum-of-products
  - newer PALs have selectable inversion
    - GAL16V8C (next slide)

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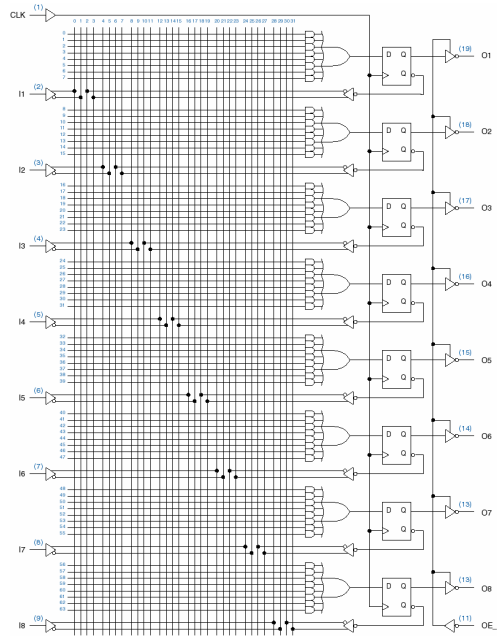


- GAL16V8C
  - 16 total inputs
  - 8 total outputs
- Selectable output inversion
  - The XOR can be used to either *pass* (programmable input = 0) or *complement* (programmable input = 1) the value out of the OR gate
- Six outputs (IO<sub>n</sub>) are "bidirectional"
  - Can be used as inputs

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## Sequential PALs

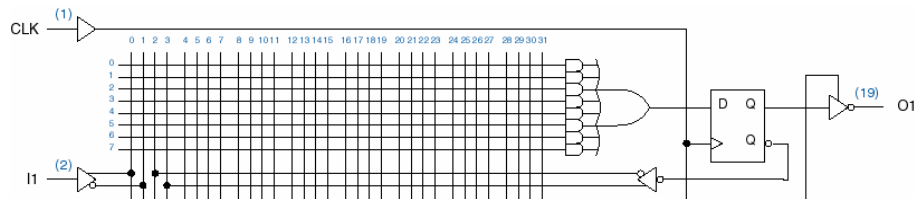
- 16R8
  - 16 total inputs
  - 8 total outputs
- Outputs are “registered”



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7

## One Output of 16R8



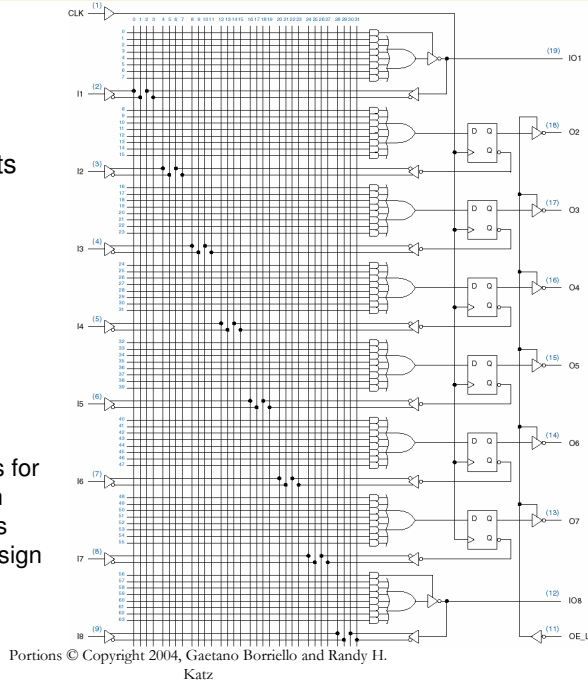
- 8 product terms to D input of flip-flop
  - positive edge triggered, common clock for all
- Q output is fed back into AND array
  - needed for state machines and other applications
- Common 3-state enable for all output pins

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8

## PAL16R6

- 6 registered outputs
- 2 combinational outputs (like the 16L8's)
  - Two bidirectional outputs
- 16 inputs
  - 8 combinational inputs
  - 8 feedback inputs for sequential design and for multi-pass combinational design



## PLD Options

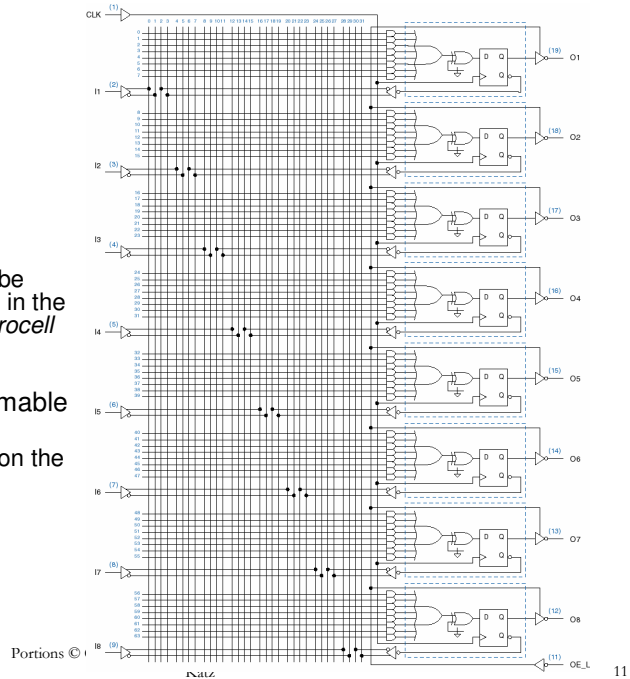
- PLDs come in a variety of configurations
- Each of the PAL16xx parts below uses the same AND-OR array, but with differing numbers of inputs and outputs (combinational versus registered)

Table 8-9 Characteristics of standard bipolar PLDs.

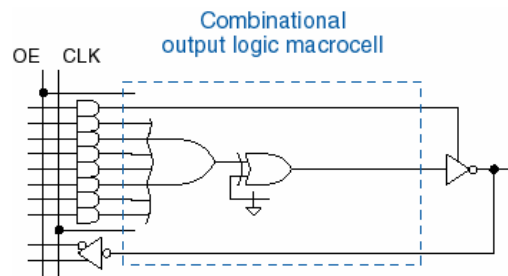
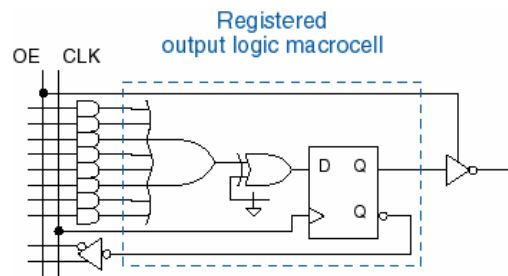
Part number	Package pins	AND-gate inputs	Inputs to AND array			
			Primary inputs	Bidirectional combinational outputs	Registered outputs	Combinational outputs
PAL16L8	20	16	10	6	0	2
PAL16R4	20	16	8	4	4	0
PAL16R6	20	16	8	2	6	0
PAL16R8	20	16	8	0	8	0
PAL20L8	24	20	14	6	0	2
PAL20R4	24	20	12	4	4	0
PAL20R6	24	20	12	2	6	0
PAL20R8	24	20	12	0	8	0

# GAL16V8

- Each output is programmable as combinational or registered
  - The flip flop can be made to "vanish" in the *output logic macrocell* under "program" control
- Also has programmable output polarity
  - Due to the XOR on the "D" input

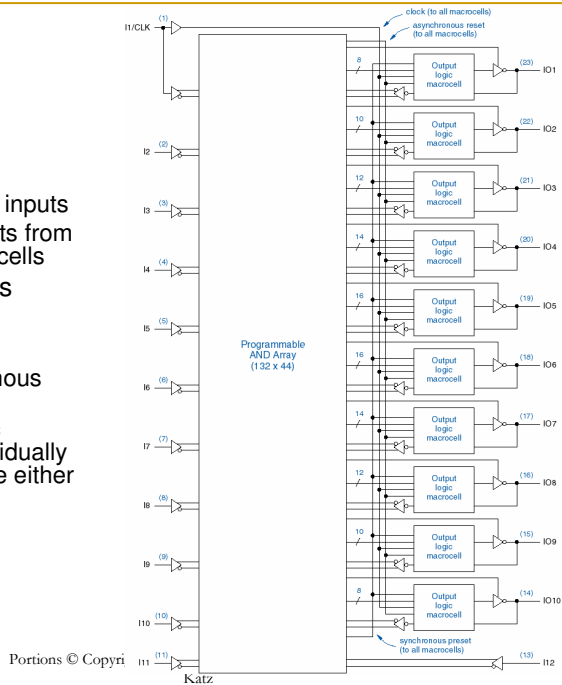


# GAL16V8 Output Logic Macrocell



# GAL22V10

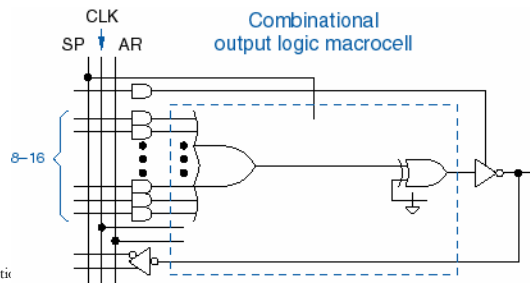
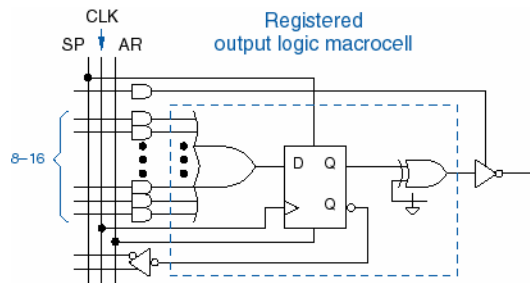
- More inputs (22)
  - 12 combinational inputs
  - 10 feedback inputs from the output macrocells
- More product terms
  - Up to 16
- More flexibility
  - Global asynchronous reset and preset
  - Each output logic macrocell is individually configurable to be either combinational or registered



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# GAL22V10 Output Logic Macrocell

**Up to 16 product terms on two pins; 8 on the others**



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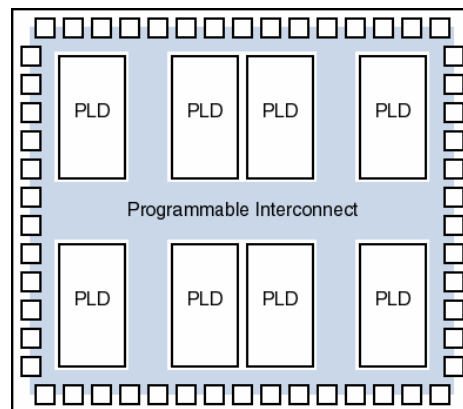
## How to expand the PLD architecture

### Why not just make really big PLDs?

- Increase # of inputs and outputs in a conventional PLD?
  - E.g., 16V8 --> 20V8 --> 22V10.
  - Why not --> 32V16 --> 128V64 ?
- Problems:
  - $n$  times the number of inputs and outputs requires  $n^2$  as much chip area -- too costly
  - logic gets slower as number of inputs to AND array increases
    - 128V64 would have 256 inputs per AND gate
- Solution: multiple PLDs with a relatively small programmable interconnect.
  - Less general than a single large PLD, but can use software “fitter” to partition into smaller PLD blocks.
  - The idea is to partition a design into several communicating pieces, each of which can be implemented in a single PLD
  - The interconnection hardware is the key!

## CPLDs

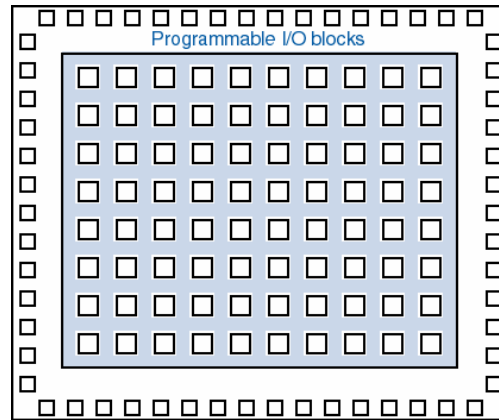
- CPLD architecture
- Small number of largish PLDs (e.g., “36V18”) on a single chip
- Programmable interconnect between PLDs



□ = input/output block

## FPGAs

- FPGA architecture
- = Programmable interconnect
- = Programmable logic block
- = I/O pad
- Much larger number of smaller programmable logic blocks.
- Embedded in a sea of lots and lots of programmable interconnects.



## CPLD Families

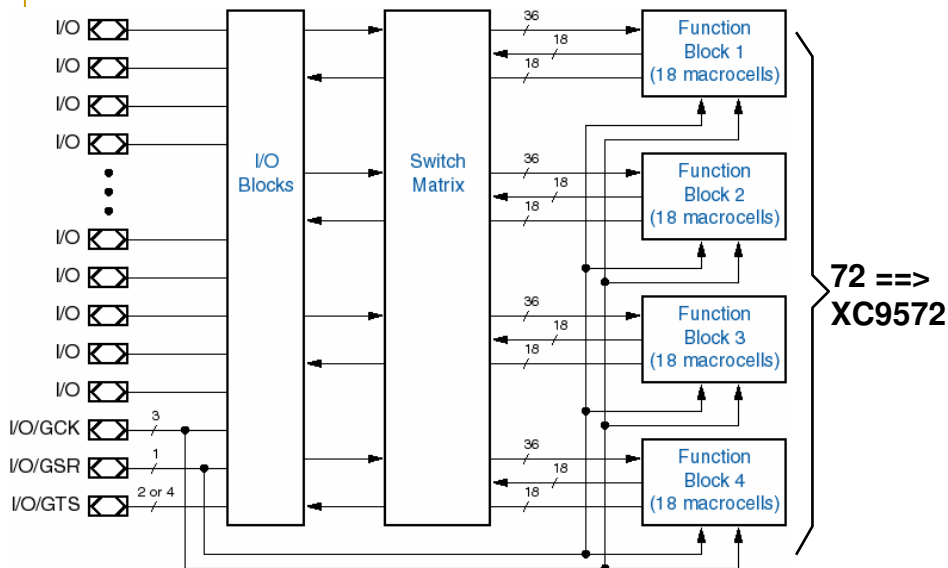
- Identical individual PLD blocks (Xilinx "FBs") replicated in different family members.
  - Different number of PLD blocks
  - Different number of I/O pins
- Many CPLDs have fewer I/O pins than macrocells
  - "Buried" Macrocells -- provide needed logic terms internally but these outputs are not connected externally.
  - IC package size dictates # of I/O pins but not the total # of macrocells.

## Xilinx CPLDs

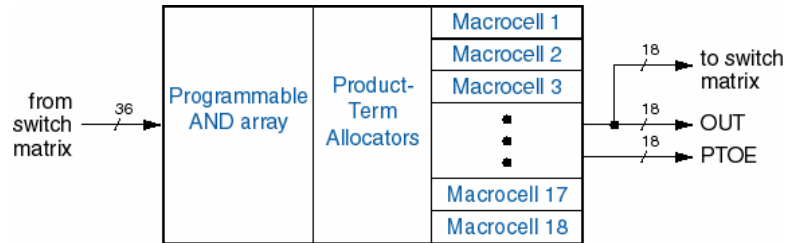
	Part Number					
	<i>XC9536</i>	<i>XC9572</i>	<i>XC95108</i>	<i>XC95144</i>	<i>XC95216</i>	<i>XC95288</i>
FBs / macrocells	2 / 36	4 / 72	6 / 108	8 / 144	12 / 216	16 / 288
<b>Package</b>	<b>Device I/O Pins</b>					
44-pin VQFP	34					
44-pin PLCC	34	34				
48-pin CSP	34					
84-pin PLCC		69	69			
100-pin TQFP		72	81	81		
100-pin PQFP		72	81	81		
160-pin PQFP			108	133	133	
208-pin HQFP					166	168
352-pin BGA					166	192

- Notice overlap in resource availability in a particular package.

## Xilinx 9500-Family CPLD Architecture



## 9500-Family Function Blocks (FBs)

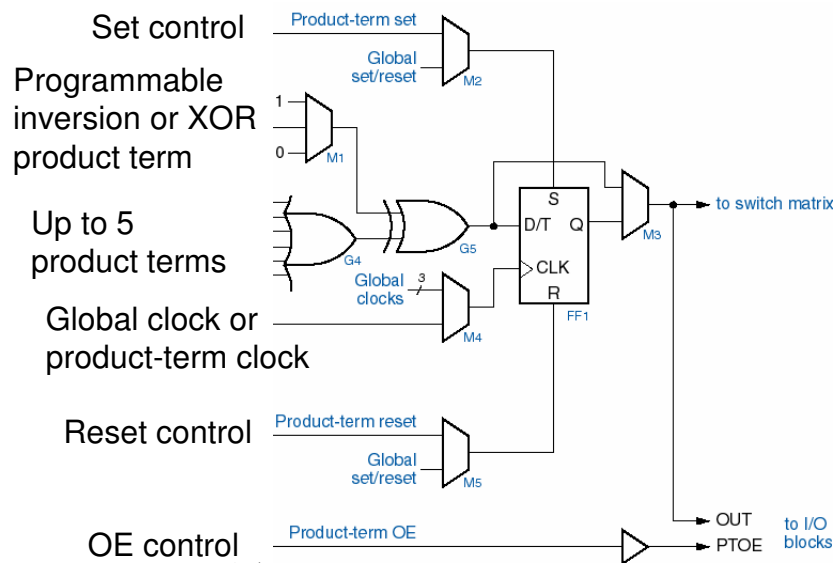


- 18 macrocells per FB
- 36 inputs per FB (partitioning challenge, but also reason for relatively compact size of FBs)
- Macrocell outputs can go to I/O cells or back into switch matrix to be routed to this or other FBs.

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21

## 9500-series Macrocell (18 per FB)

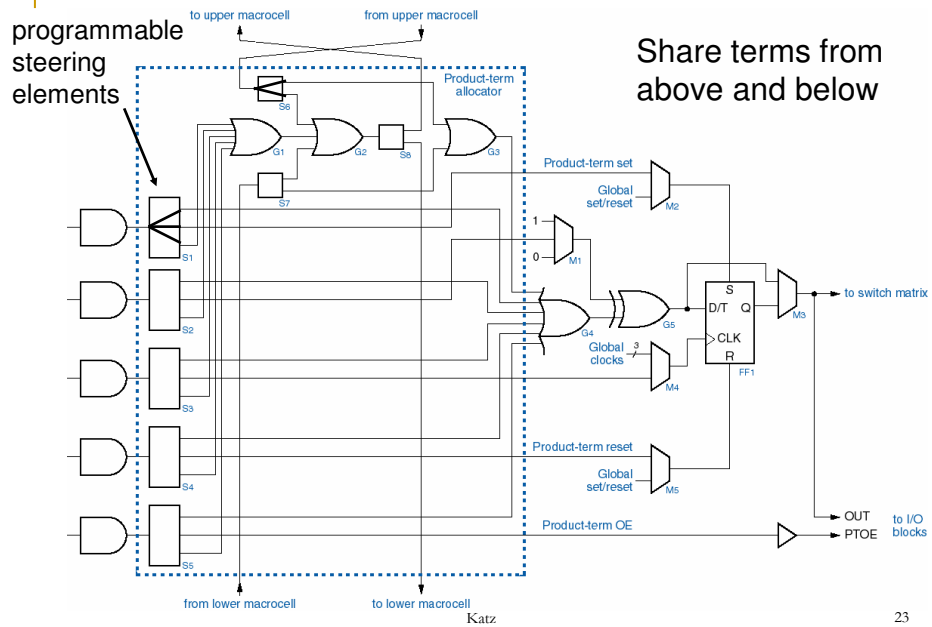


Portion

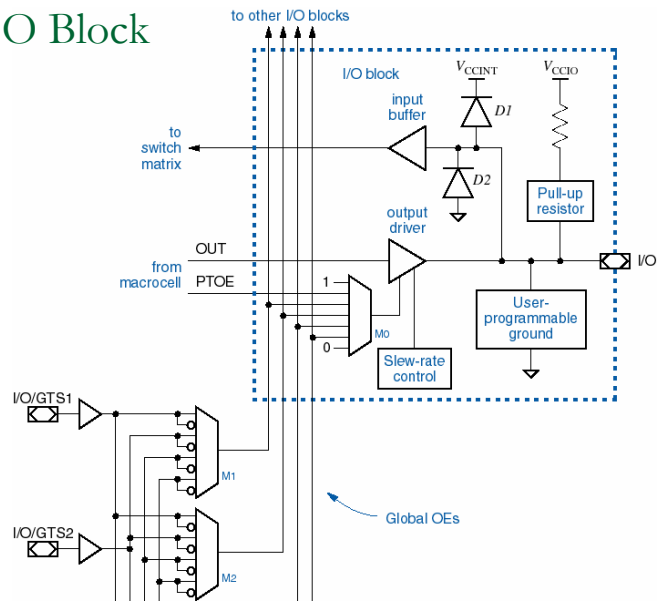
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22

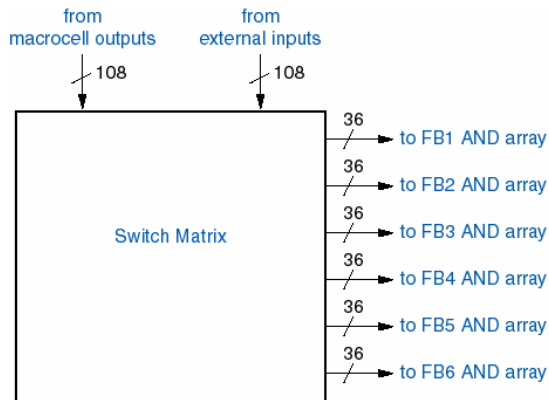
## 9500-Series Product-Term Allocator



## 9500-Series I/O Block



## Switch Matrix for XC95108

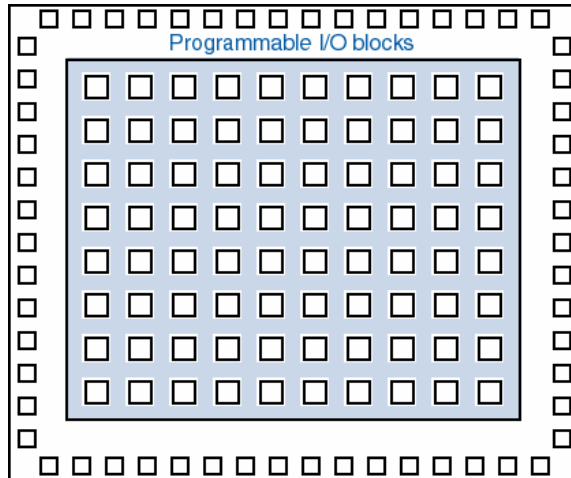


- Could be anything from a limited set of multiplexers to a full crossbar.
- Multiplexer -- small, fast, but difficult fitting
- Crossbar -- easy fitting but large and slow

## FPGAs

- Historically, FPGA architectures and companies began around the same time as CPLDs
- FPGAs are closer to "programmable ASICs" -- large emphasis on interconnection routing
  - Timing is difficult to predict -- multiple hops vs. the fixed delay of a CPLD's switch matrix.
  - But more "scalable" to large sizes.
- FPGA programmable logic blocks have only a few inputs and 1 or 2 flip-flops, but there are a lot more of them compared to the number of macrocells in a CPLD.

## General FPGA chip architecture



- = Programmable interconnect
- = Programmable logic block
- = I/O pad

a.k.a. CLB --  
“configurable logic  
block”

## Xilinx 4000-series FPGAs

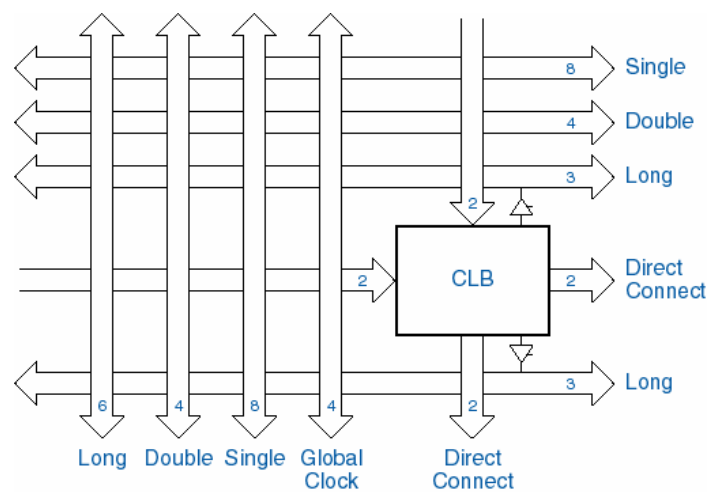
Device	CLB Matrix	Total CLBs	Max. User I/O	Flip-Flops	Max. RAM bits (no logic)	Max. Gates (no RAM)	Typical Gate Range (Logic and RAM)
XC4002XL	8×8	64	64	256	2,048	1,600	1,000–3,000
XC4003E	10×10	100	80	360	3,200	3,000	2,000–5,000
XC4005E/XL	14×14	196	112	616	6,272	5,000	3,000–9,000
XC4006E	16×16	256	128	768	8,192	6,000	4,000–12,000
XC4008E	18×18	324	144	936	10,368	8,000	7,000–15,000
XC4010E/XL	20×20	400	160	1,120	12,800	10,000	7,000–20,000
XC4013E/XL	24×24	576	192	1,536	18,432	13,000	10,000–30,000
XC4020E/XL	28×28	784	224	2,016	25,088	20,000	13,000–40,000
XC4025E	32×32	1,024	256	2,560	32,768	25,000	15,000–45,000
XC4028EX/XL	32×32	1,024	256	2,560	32,768	28,000	18,000–50,000
XC4036EX/XL	36×36	1,296	288	3,168	41,472	36,000	22,000–65,000
XC4044XL	40×40	1,600	320	3,840	51,200	44,000	27,000–80,000
XC4052XL	44×44	1,936	352	4,576	61,952	52,000	33,000–100,000
XC4062XL	48×48	2,304	384	5,376	73,728	62,000	40,000–130,000
XC4085XL	56×56	3,136	448	7,168	100,352	85,000	55,000–180,000



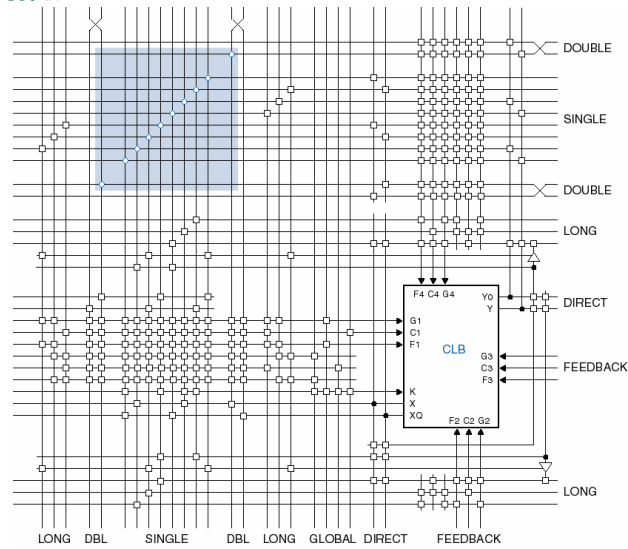
## CLB Function Generators (F, G, H)

- Use RAM to store a truth table
  - F, G: 4 inputs, 16 bits of RAM each
  - H: 3 inputs, 8 bits of RAM
  - RAM is loaded from an external PROM at system initialization.
- Broad capability using F, G, and H:
  - Any 2 functions of 4 variables, plus a function of 3 variables
  - Any function of 5 variables
  - Any function of 4 variables, plus some functions of 6 variables
  - Some functions of 9 variables, including parity and 4-bit cascadable equality checking

## CLB input and output connections -- buried in the sea of interconnects

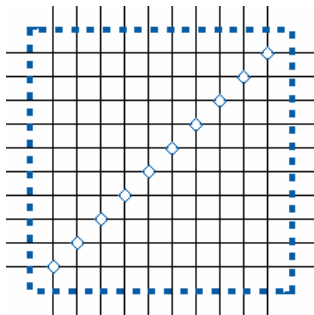


## Detail

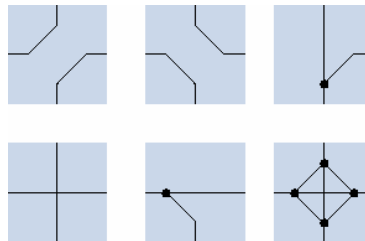
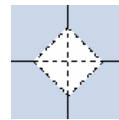


connections controlled by RAM bits

## Programmable Switch Matrix



programmable switch element

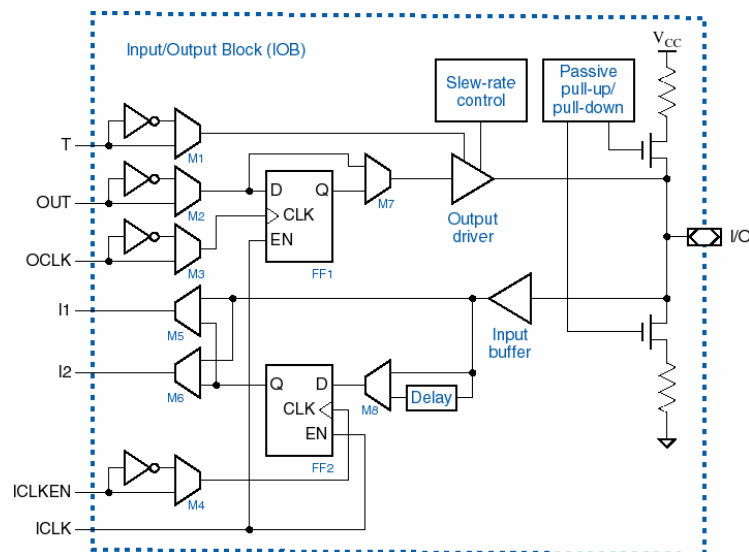


turning the corner, etc.

## The Fitter's Job

- Partition logic functions into CLBs
- Arrange the CLBs
- Interconnect the CLBs
- Minimize the number of CLBs used
- Minimize the size and delay of interconnect used
- Work with constraints
  - "Locked" I/O pins
  - Critical-path delays
  - Setup and hold times of storage elements

## I/O Blocks



## Summary

- PLA/PAL
- CPLD
- FPGA