

Full Name: Bobl Pste

Digital Logic Design, Fall 2008

Final Exam

~~May 1, 2008~~

Instructions:

- Make sure that your exam is not missing any sheets, then write your full name on the front.
- Write your answers in the space provided below the problem. If you make a mess, clearly indicate your final answer.
- The exam has a maximum score of 220 points.
- You have 1 hour and 50 minutes to complete this exam.
- The problems are of varying difficulty. The point value of each problem is indicated. Pile up the easy points quickly and then come back to the harder problems.
- The bonus questions discussed in class are the ones with the asterix next to them. To receive the bonus for test 2, you must get both of these problems completely correct to get the bonus for test 2.
- This exam is CLOSED BOOK. You are only allowed to use the single sheet (front and back) of notes you made for this exam. Please hand in this sheet along with your test. If you did not use a sheet, just hand in a blank piece of paper with your name on it. Good luck!

1 (40):
2 (30):
3 (50) [*]:
4 (50) [*]:
5 (20):
6 (30):
TOTAL (220):

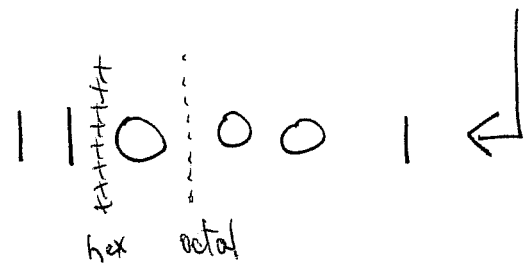
Problem 1. (40 points):

Determine the unsigned binary, octal, hexadecimal representation of the number 49_{10} .

- Binary:
- Octal:
- Hex:

2^i	2^i
0	1
1	2
2	4
3	8
4	16
5	32

$$49 = 32 + 16 + 1$$



$$\text{Binary} = 110001_2$$

$$\text{Octal} = 61_8$$

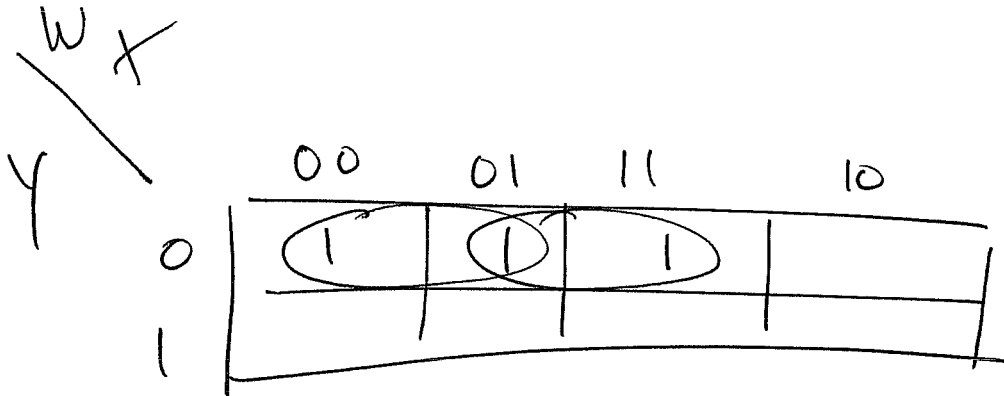
$$\text{Hex} = 31_{16} = \text{x}31$$

Problem 2. (30 points):

Write the corresponding minimum sum of products (MSOP) solution to the following truth table with inputs W, X, Y and output Z .

W	X	Y	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Table 1: Problem 2 - Truth Table.



$$Z = \overline{w} \overline{y} + x \cdot \overline{y} = \overline{y} (\overline{w} + x)$$

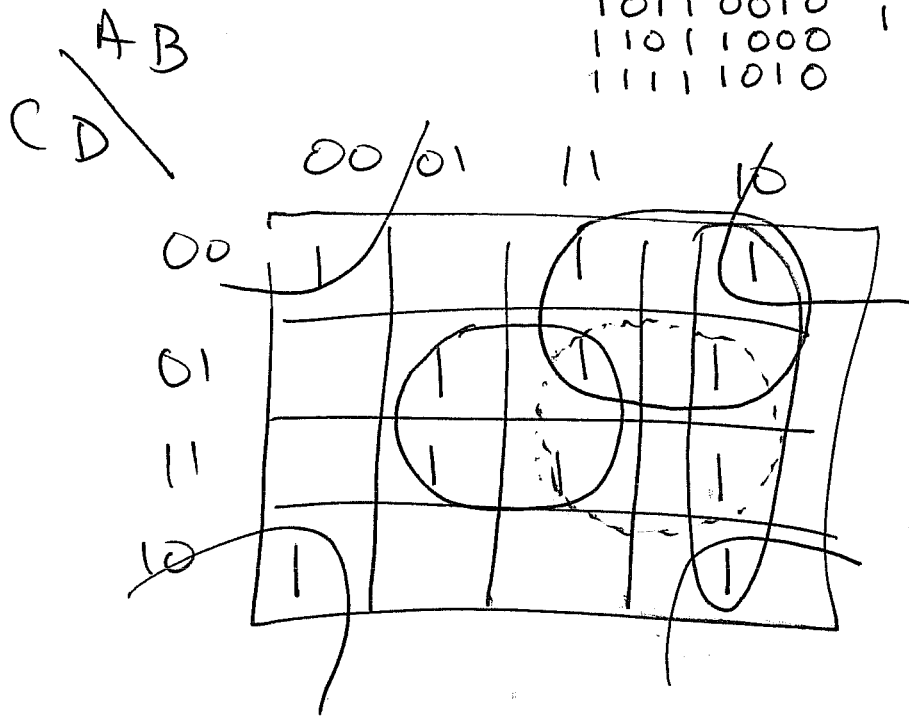
Problem 3. (50 points):

Joe has tried to minimize a Boolean equation and he has come up with the solution listed below. However, you notice that these equations are not minimal. Using a K-map, find the minimal representation of this equation.

$$Y = (\bar{A} \cdot B \cdot C \cdot D) + (A \cdot B \cdot \bar{C} \cdot \bar{D}) + (A \cdot D) + (\bar{B} \cdot \bar{D}) + (B \cdot \bar{C} \cdot D)$$

0111, 1100, 1XX1, X0X0, X101

1001	0000	0101
1011	0010	1001
1101	1000	
1111	1010	



$$Y = \bar{B}\bar{D} + BD + A\bar{C} + A\bar{B}$$

Problem 4. (50 points):

Figure 1 shows a Finite State Machine diagram. This FSM diagram is a specialized finite state machine with one input E , and one output Z . Design a complete implementation of a Finite State Machine assuming the following encoding values for each state: $P = 000$, $I = 001$, $S = 010$, $T = 011$, $O = 100$ and $L = 101$. All states that are not encoded should be entered in as don't care entries. You can assume that this design uses resettable flip-flops. That is, **do not incorporate a reset input, except to have one tied to the reset input of each flip-flop**. Is this a Mealy or Moore Finite State Machine? What are the advantages and disadvantages of Moore vs. Mealy Finite State machines. Please explain your reasoning.

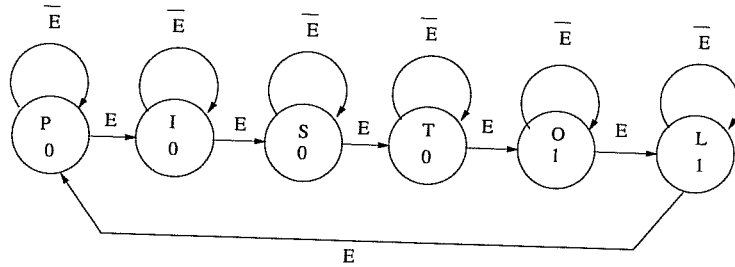


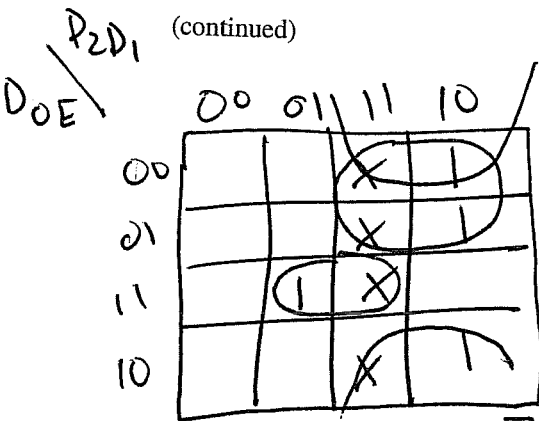
Figure 1: Problem 4.

C.S	Input	N.S	Output
P	0	P	0
P	1	I	0
I	0	I	0
I	1	S	0
S	0	S	0
S	1	T	0
T	0	T	0
T	1	O	0
O	0	O	1
O	1	L	1

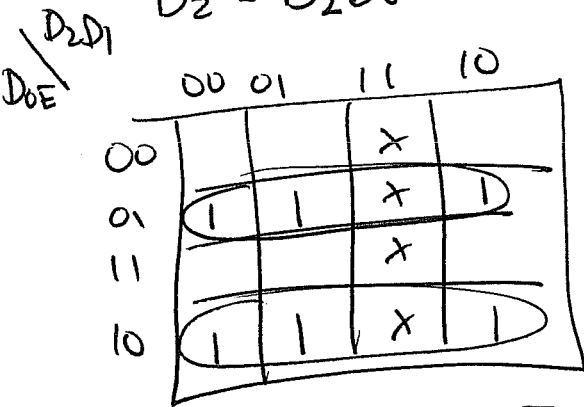
Cs	In	NS	Output
L	0	L	1
L	1	P	1

(continued)

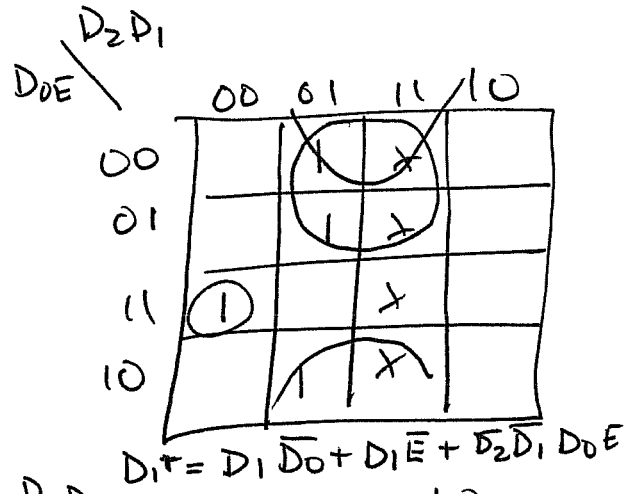
Current State			Input	Next State			output
D_2	D_1	D_0	E	D_2^*	D_1^*	D_0^*	Z
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	0
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	0
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	1
1	0	1	0	1	0	1	1
1	0	1	1	0	0	0	1
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x



$$D_2^* = D_2 \bar{D}_0 + D_2 \bar{E} + D_1 D_0 E$$



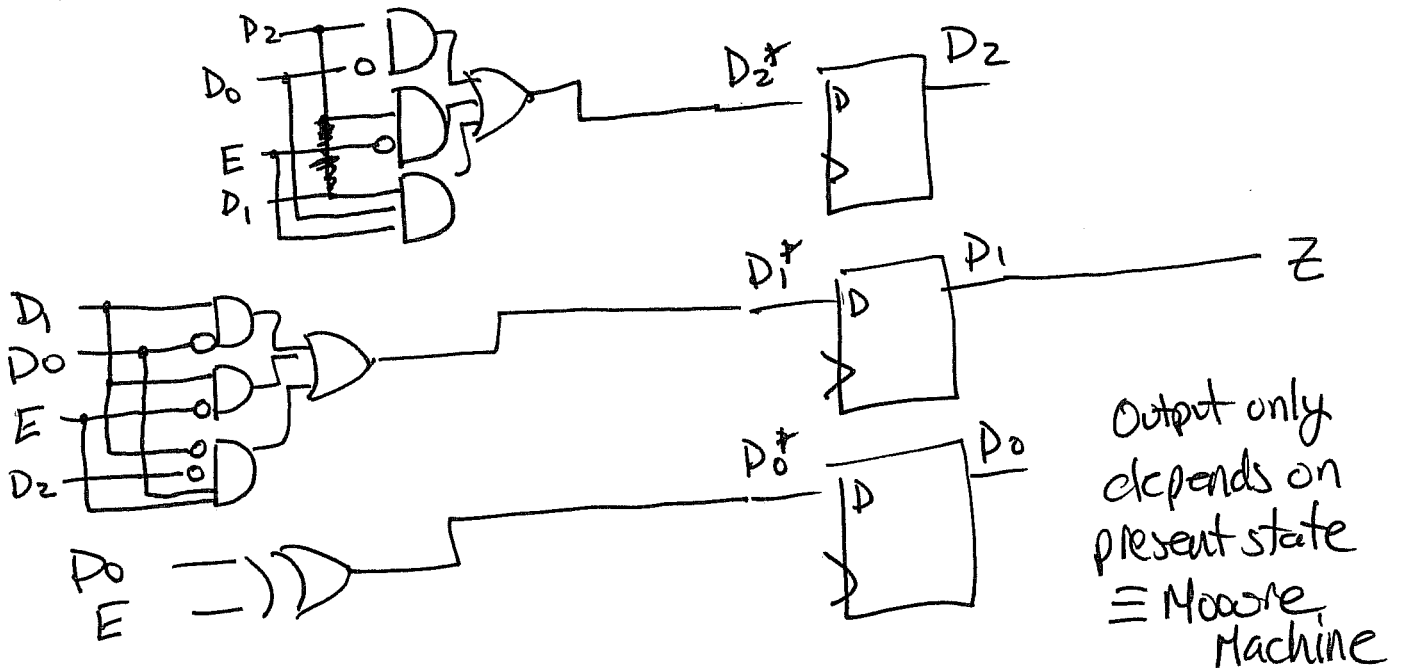
$$D_0^* = \bar{D}_0 E + D_0 \bar{E} = D_0 \oplus E$$



$$D_1^* = D_1 \bar{D}_0 + D_1 \bar{E} + D_2 \bar{D}_1 D_0 E$$



$$Z = D_2$$

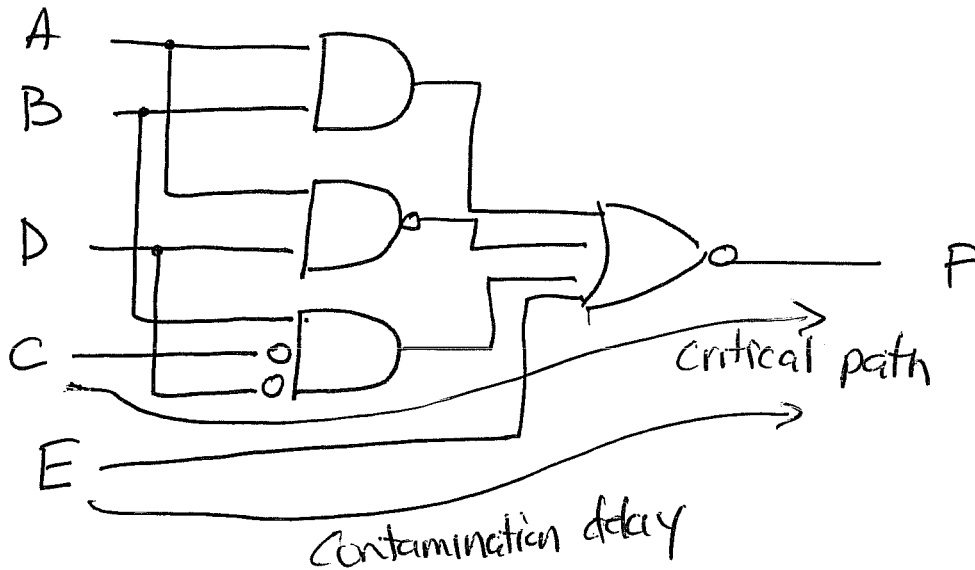


- Moore machines have more states
- Mealy machines output their value

Problem 5. (20 points):

Show a schematic for the following equation. Assuming each gate takes the same delay, highlight the critical path and contamination delay on the schematic. Write a Verilog implementation for this circuit, as well.

$$F = \overline{(A \cdot B) + \overline{A} \cdot \overline{D} + (B \cdot \overline{C} \cdot \overline{D})} + E$$



```
module prob5(input A,B,C,D,E, output F) ;
```

```
assign F = ~( (A&B) | (~(A&D)) | (B&~C&~D) ) | E;
```

```
endmodule
```

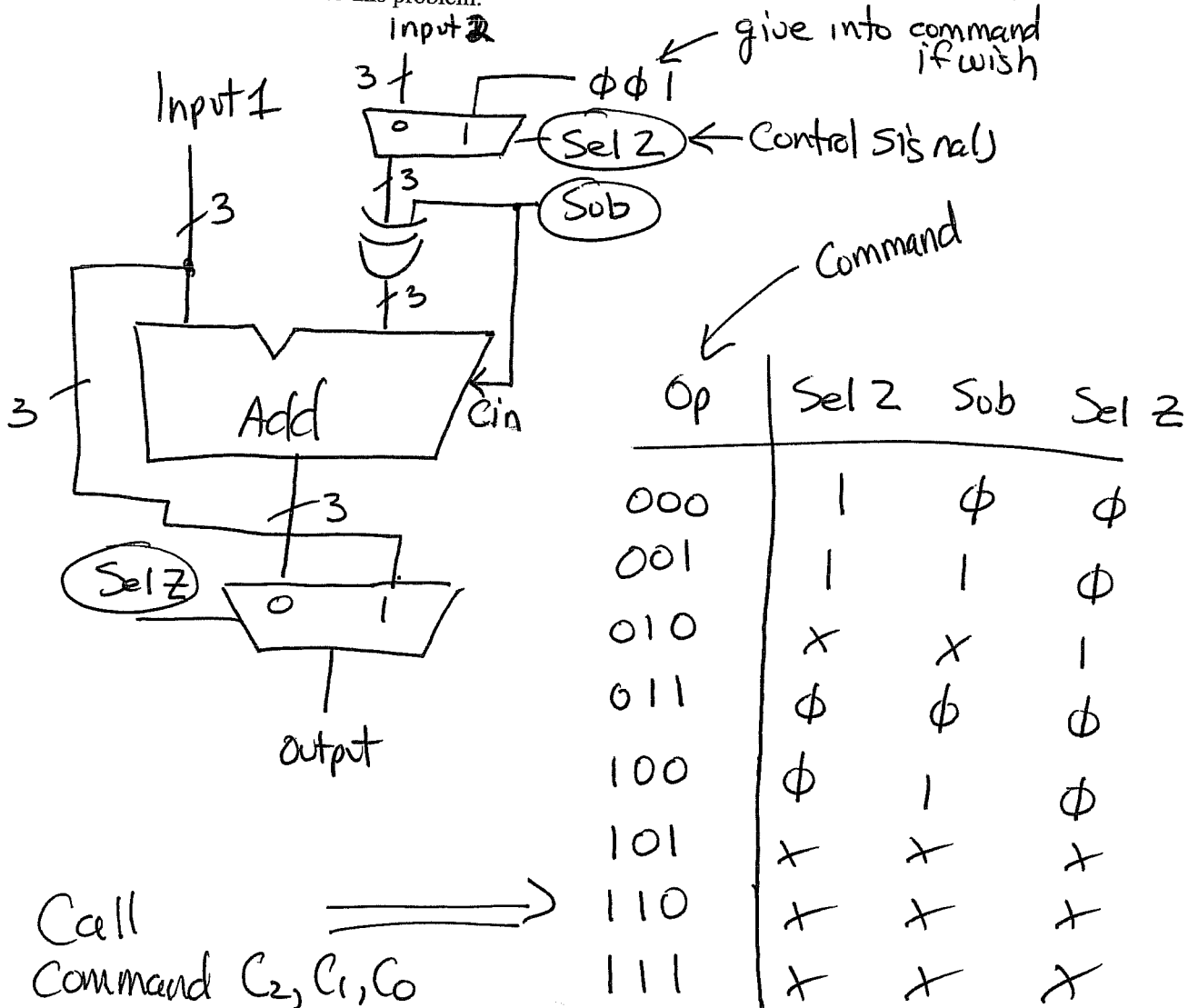
Problem 6. (30 points):

Walmart is excited to hear that you graduated from Oklahoma State University and they are eager to have you redesign a new digital device called GundyCalc that they believe is going to be a best seller (and, of course, reward you for your efforts). The new digital device has several functions assuming the device accepts 2 input operands of 3 bits each and a command (you can encode this any way you want). The following commands need to be designed for GundyCalc:

- 000 • Output = Input1 + 1
- 001 • Output = Input1 - 1
- 010 • Output = Input1
- 011 • Output = Input1 + Input2
- 100 • Output = Input1 - Input2

One potential solution given below

Design the digital logic for this part. Please also document the command structure for this digital logic. There are various correct solutions to this problem.



(continued)

$C_2 C_1$				
C_0	00	01	11	10
0	1	X	X	
1	1		X	X

$$Sel Z = \overline{C_2} \overline{C_1}$$

$C_2 C_1$				
C_0	00	01	11	10
0		X	X	1
1	X		X	X

$$Sub = C_2 + \overline{C_1} C_0$$

$C_2 C_1$				
C_0	00	01	11	10
0		1	X	
1			X	X

$$Sel Z = C_1 \overline{C_0}$$

Command Structure

