Name_____

Digital Logic Design
ECEN 3233

Exam 2
Spring 2003

Closed Book
One page, single sided, handwritten, original notes allowed

This exam consists of seven problems on seven pages
including the cover sheet. Be sure you have all the problems.

Write neatly, and clearly indicate each answer
by enclosing it in a box.

Show all your work for partial credit.

Start and stop work as instructed.

Do your own work!

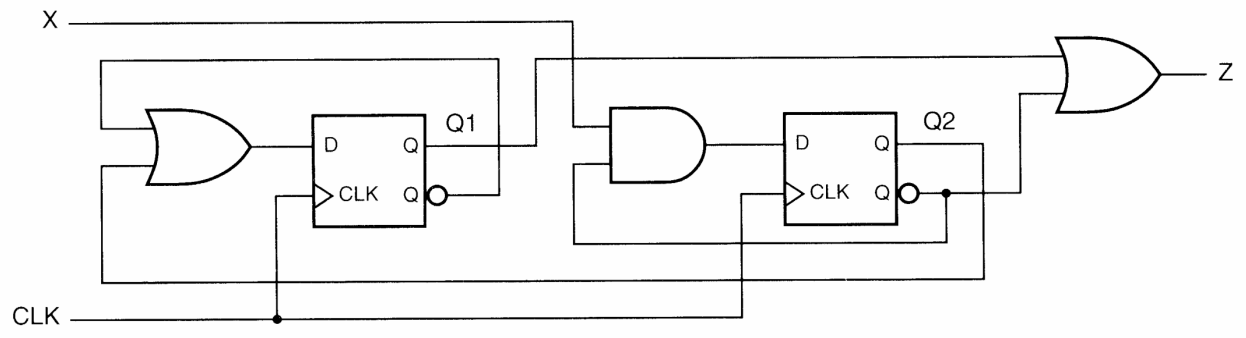
Name_____

1. (20 points). Circle **T**rue or **F**alse.

T	F	A sequential machine with four states and two inputs will have at most four transition arrows leaving any particular state.
T	F	A T flip-flop can be implemented using a J-K flip-flop with the J and K inputs tied to ground.
T	F	A 16:1 multiplexer has three select inputs.
T	F	Steering logic can be constructed from CMOS transmission gates.
T	F	A clocked sequential circuit can be made to operate slower by using flip-flops with a longer setup time.
T	F	The Xilinx FPGA you are using in lab is the XC2S50 Spartan II device.
T	F	The frequency of oscillation of a ring oscillator constructed from an odd number of inverters is affected by the propagation delay of each inverter and the capacitance in the circuit.
T	F	Under the right conditions, the outputs of *tri-state* or *open-collector* devices can be tied together without damage.
T	F	One-hot encoding requires fewer flip-flops than straight binary encoding.
T	F	The D flip-flop is your friend!

Name_____

2. (8 points) Consider the clocked synchronous state machine shown below. The input is X and the output is Z.
   a. What type of sequential machine is represented by the schematic below – Moore or Mealy? Why?
   b. How many states does the sequential machine probably have? Why?



3. (9 points) Short Answer.

   a. A sequential circuit is to output a ONE when an even number (≥ 0) of ones are input; otherwise the output is ZERO. The minimum number of states required is:_____.

   b. If you were to build a 64:1 multiplexer from several 4:1 multiplexers and no other logic, how many 4:1 multiplexers would you need? _____

   c. A 74LS74 is an example of a(n) _____.

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4. (16 points) Design a circuit using edge triggered JK flip-flops to realize the state transition table below. Complete the table and determine the minimized excitation equation(s). Use only AND, OR and INVERT gates as needed. The output is Q. Do not perform state reduction. It's not necessary to draw the circuit. Be sure to use *don't cares* where appropriate. Show your work. This is a Moore machine.

Present State	Input	Next State	Excitation	
Q	I	Q+	J	K
0	0	0		
	1	1		
1	0	1		
	1	1		

Name_____

5. (16 points) A combinational circuit has inputs **A**, **B** and **C**. The output is **OUT**. A truth table is shown below.

   Implement the **OUT** output function of this circuit by using a single 4:1 multiplexer and no additional logic. Assume that the input variables, their complements, 1 and 0 are available to use as inputs. Use **B** and **C** as select inputs. Sketch the circuit (represent the multiplexer as a simple rectangular block with appropriate inputs and outputs) and clearly label the connections. Show all of your work.

A	**B**	**C**	**OUT**
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Name_____

6. (16 points) The state transition table for a finite state machine is given below.

   Determine the excitation equation(s) to implement this finite state machine using edge triggered D flip-flop(s). The equations should be *minimized* and written in *sum-of-products* form (AND, OR and INVERT operations only on variables and their complements). Do NOT try to reduce the states! There is no output equation. Show all your work. It's <u>not</u> necessary to draw the final circuit.

Present State		**Next State**
(Q1,Q0)	**Input**	**(Q1+,Q0+)**
0 0	**0**	**0 1**
	1	**1 1**
0 1	**0**	**1 0**
	1	**0 0**
1 0	**0**	**1 1**
	1	**0 1**
1 1	**0**	**0 0**
	1	**1 0**

Name_____

7. (15 points) Draw a state diagram for the sequential circuit below. Clearly label the state diagram. Indicate the transitions using the notation (In1, In2) to indicate the condition on each transition arrow, where the values inside the parentheses are binary numbers. In1 and In2 are circuit inputs, and Out is the circuit output. Assume the flip-flop is an edge-triggered D type device.